$Al/Cu_xO/Cu$ Memristive Devices:

Fabrication, Characterization, and Modeling

by

Nathan R. McDonald

A Thesis

Submitted to the University at Albany, State University of New York

in Partial Fulfillment of

the Requirements for the Degree of

Master of Science

College of Nanoscale Science & Engineering

Department of Nanoscale Engineering

2012

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
25 JUL 2012	**N/A**	**01 SEP 2010 - 01 Jul 2012**

4. TITLE AND SUBTITLE
Al/CuxO/Cu Memristive Devices: Fabrication, Characterization, and Modeling

5a. CONTRACT NUMBER
5b. GRANT NUMBER
5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Nathan R. McDonald

5d. PROJECT NUMBER
5e. TASK NUMBER
5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
AFRL Information Directorate

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory Information Directorate, 525 Brooks Rd, Rome, NY 13441

10. SPONSOR/MONITOR'S ACRONYM(S)
11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
PA: 88ABW-2012-3934, The original document contains color images.

14. ABSTRACT
Memristive devices have become very popular in recent years due to their potential to dramatically alter logic processing in CMOS circuitry. Memristive devices function as electrical potentiometers, allowing for such diverse applications as memory storage, multi-state logic, and reconfigurable logic gates. This research covered the fabrication, characterization, and modeling of Al/CuxO/Cu memristive devices created by depositing Al top electrodes atop a CuxO film grown using plasma oxidation to grow the oxide on a Cu wafer. Power settings of the plasma oxidation system were shown to control the grown oxide thickness and oxygen concentration, which subsequently affected memristive device behaviors. These memristive devices demonstrated complete nonpolar behavior and could be switched either in a vertical (Al/CuxO/Cu) or lateral (Al/CuxO/Cu/CuxO/Al) manner. The switching mechanism of these devices was shown to be filamentary in nature. Physical and empirical models of these devices were created for MATLAB, HSPICE, & Verilog A environments. While the physical model proved of limited practical consequence, the robust empirical model allows for rapid prototyping of CMOS-memristor circuitry.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**124**	

The views expressed in this thesis are those of the author and do not reflect the official policy or position of the United States Air Force, Department of Defense, or the U.S. Government.

Abstract:

Memristive devices have become very popular in recent years due to their potential to dramatically alter logic processing in CMOS circuitry. Memristive devices function as electrical potentiometers, allowing for such diverse applications as memory storage, multi-state logic, and reconfigurable logic gates.

This research covered the fabrication, characterization, and modeling of Al/Cu_xO/Cu memristive devices created by depositing Al top electrodes atop a Cu_xO film grown using plasma oxidation to grow the oxide on a Cu wafer. Power settings of the plasma oxidation system were shown to control the grown oxide thickness and oxygen concentration, which subsequently affected memristive device behaviors. These memristive devices demonstrated complete nonpolar behavior and could be switched either in a vertical (Al/Cu_xO/Cu) or lateral (Al/Cu_xO/Cu/Cu_xO/Al) manner. The switching mechanism of these devices was shown to be filamentary in nature.

Physical and empirical models of these devices were created for MATLAB, HSPICE, & Verilog A environments. While the physical model proved of limited practical consequence, the robust empirical model allows for rapid prototyping of CMOS-memristor circuitry.

Acknowledgements:

I would like to express my sincere thanks to my advisor Dr. Nathaniel Cady for his guidance and support. I would also like to thank Seann Bishop for his time and assistance at all stages of this research. I would also like to thank Dr. Joseph Van Nostrand for all his guidance with this project. I would also like to thank Dr. Bryant Wysocki & Thomas McEwen for all their technical assistance and encouragement.

Finally, I want to thank my parents for all their love and encouragement these past couple years.

Table of Contents:

List of Figures:

List of Tables:

I. Introduction

Memristive devices are two terminal, electrical potentiometers. That is, they behave as non-volatile, variable resistors whose resistance is modulated by a voltage bias. As such, these devices have the potential to become a game changing technology. With respect to traditional von Neumann computing, these devices may be employed as memory cells or strategically incorporated into circuits to create reconfigurable logic gates [1-3]. Additionally, memristive devices function as the hardware equivalent of a biological synapse [4], and thus, may be an enabling technology for neuromorphic computing at a biological systems scale.

In practice, memristive devices may be created from as few as three material layers, metal-insulator-metal (MIM). However, with respect to complementary metal-oxide-semiconductor (CMOS) technology, only certain materials are allowed in the front-end-of-line (FEOL) and the back-end-of-line (BEOL). Cu is ubiquitous in the BEOL, and metal/Cu_xO/Cu memristive devices have been reported in the literature [5-7].

The research presented herein demonstrated the plasma oxidation power correlation with final oxide layer thickness and oxygen concentration. Complete nonpolar switching behavior was observed in Al/Cu_xO/Cu memristive devices fabricated for this research. Various switching mechanisms have been reported for Cu_xO based memristive devices due to processing variations of the oxide layer. For the devices prepared for this research, the switching mechanism was shown to be filament formation, where filament composition modulation was suggested to be source of the complete nonpolar bistable

switching. These observations provide a foundation for future device engineering for application specific circuit hardware, e.g. resource constrained platforms.

This document is composed of six chapters. Of the remaining chapters, Chapter 2 covers the detailed history of the memristive device, from its theoretical conception to its physical inception. An overview of the materials and methods used in this research are provided in Chapter 3. Chapter 4 presents the characterization data and analysis. Physical and empirical models of memristive device behavior for incorporation with circuit simulation software are covered in Chapter 5. Finally, a summary of the research conclusions and planned future research are addressed in Chapter 6.

II. Background

2.1 Memristor Theory

Traditionally, circuit theory is governed by four fundamental variables and five relationships between the aforesaid variables. These fundamental variables are electric current i, voltage v, electric charge q, and magnetic flux φ. The first two relationships concern current and magnetic flux. Current is the time integral of electric charge, $dq = i\,dt$. Magnetic flux is the time integral of voltage, $d\varphi = v\,dt$. The other three relationships are physically realized as the fundamental passive circuit elements, viz. resistor (1745), $dv = R\,di$; capacitor (1827), $dq = C\,dv$, and inductor (1831), $d\varphi = L\,di$.

In 1971, Leon Chua predicted the existence of a fourth fundamental circuit element in his paper "Memristor - The Missing Circuit Element." [8] When these five electronics equations were arranged graphically, symmetry seemed to suggest the existence of a device to relate magnetic flux to charge, $d\varphi = M\,dq$ (Figure 2.1.1). Although nature required no symmetry *per se*, in the grand tradition of Dmitri Mendeleev, Chua mathematically described the properties that such a device would possess.

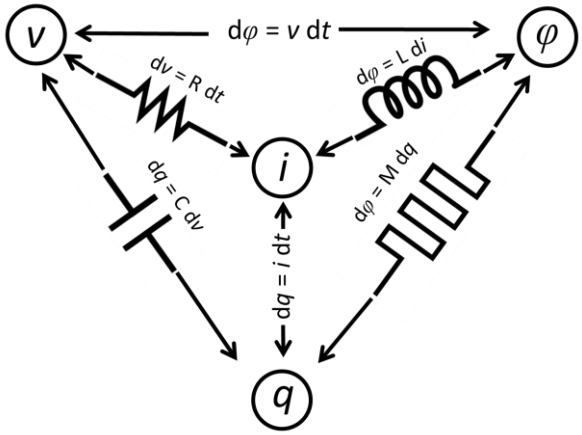


Figure 2.1.1 This figure shows the relationships between the four fundamental circuit variables and their respective relationships between each other.

In one algebra step, the d$\varphi = M$ dq relation becomes a variant of Ohm's Law,

$$M\left(q(t)\right) = \frac{d\varphi/dt}{dq/dt} = \frac{V(t)}{I(t)}. \tag{2.1.1}$$

Understood in this way, M then has units of ohms like a resistor; however, the device's resistance would not be fixed but would vary as a function of the total charge through the device. Given a sine wave input voltage, Equation 2.1.1 yielded an I-V curve of a pinched hysteresis loop odd symmetric about the origin (Figure 2.1.2). This hysteresis loop arose from the phase shift of the current through the device with respect to the applied voltage bias. The loop was pinched at the origin because $I = 0$ when $V = 0$ from Equation 2.1.1. Still further, this indicated that the device was purely dissipative; and energy was not required for the device to "remember" its current resistance value [9]. Thus, Chua named his theoretical device a "memristor," a portmanteau of "memory resistor," and the M from his equation "memristance" for "memory resistance" [9]. He considered his device the fourth fundamental passive circuit element because no

combination of nonlinear resistors, capacitors, or inductors could replicate the predicted behaviors of the memristor [9].

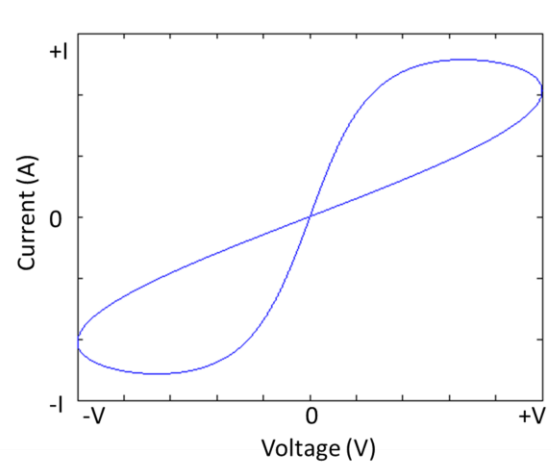


Figure 2.1.2 The I-V curve of an ideal memristor is a pinched hysteresis loop, odd symmetric about the origin which it crosses. The hysteresis loop shows that the device's resistance value is a function of its previous values. The device requires no additional energy to "remember" its current resistance value, as indicated by no current at 0 V.

Chua predicted two other properties that memristors should exhibit. With respect to physical device size, the memristance fell off as a $1/r^2$ relationship; thus only as devices became smaller would the memristance effect become more appreciable [3]. Lastly, since the device resistance was a function of the total charge through the device, a sine wave of the appropriate wavelength and frequency would cycle a memristor through its entire I-V curve. If the frequency was increased significantly, then the memristor would no longer be afforded sufficient time to completely cycle, which would shrink the accessible resistance range. Beyond a certain frequency, the memristor would appear to be a normal resistor [3, 10].

In 1976, Chua and his graduate student, Sung Mo Kang, expanded their memristance relation predictions to include a broader class of systems called "memristive systems." These systems are defined by the relationship $v(t) = R(w,i)\ i(t)$, where w defines the internal state of the system and $(dw/dt) = f(w,i)$ [9]. By this definition, the memristor itself was a special case of a memristive system.

Despite the detailed list of expected device behaviors, there still was difficulty in translating the mathematical memristor framework to a physical device. In particular, while in a memristive system the magnetic flux was no longer a unique function of the charge, its exact role was then unclear. These concepts and the search for the memristor fell out of general thought.

2.2 Physical Realization of the Memristor

a) Discovery

Contemporaneously, scientists began reporting anomalous resistance switching behaviors in devices. Chua's predicted pinched hysteresis loop was observed in devices made from a wide variety of materials [11-41], to include organic films [14, 16, 25, 28, 29, 37, 38], chalcogenides [23, 26, 34, 39], metal oxides [11, 12, 24, 39], and perovskites [15, 27, 30-32, 39]. Often these devices were simple metal-insulator-metal (MIM) structures. Since the theoretical memristor had not been associated with these devices at the time, these devices and their switching properties were referenced under a variety of names to include: bistable switching, nonvolatile memory, phase change memory, and resistive

random access memory (RRAM). Given the range of names for the disparate physical switching phenomena, a link across devices was not anticipated.

In 2008, Stanley Williams from Hewlett Packard (HP) announced the first memristor, a $Pt/TiO_2/TiO_{2-x}/Pt$ device, in which the mathematical theory of the memristor was explicitly used to describe the behavior of a physical device [3]. The effective transport mechanism in TiO_2 based memristors was ascribed to a positively charged oxygen vacancy drift originating within the oxygen deficient TiO_{2-x} layer [3]. Thus, under a positive voltage bias these vacancies would drift towards one end of the device decreasing the effective resistance of the memristor as time progressed. Additionally, once the voltage was removed, there would be insufficient force to cause said vacancies to move any farther. Upon the application of a negative voltage bias, the vacancies moved back whence they came, increasing the effective resistance of the memristor.

While this explanation was instructional for how to start interpreting the previously observed hysteretic behaviors, it was far from physically accurate. Similar TiO_2 memristive devices were shown to switch via phase change [42]. In other devices, filament creation and destruction [43, 44] and trap state filling/emptying [6, 15] were identified as the switching mechanism.

To account for the wide variety of switching behaviors not explicitly dependent upon the electric charge and the magnetic flux exhibited by these rediscovered memristors, Chua revised some of his descriptions of memristors. First, Chua asserted that the memristor

was not unique to any physical material or switching mechanism. Second, q & φ were merely mathematical constructs that did not need to be translated to physical properties. Thus, according to Chua [10], any two terminal, passive electronic device that may be switched between two or more resistances via the application of an appropriate voltage or current signal and whose present resistance value may be queried using a smaller "read" signal is a memristor or a memristive device, i.e., "If it's pinched, it's a memristor." [45]. Most of the physical devices described in this paper were strictly speaking memristive devices [9] and shall be referred to as such herein.

b) Typical Device Operation

The memristive device has at least two critical resistance states, a high resistance state (HRS) and a low resistance state (LRS). To change a memristive device from the HRS to the LRS (termed a SET operation), a voltage bias of the appropriate polarity and magnitude, V_{SET}, must be applied to the device. Additionally, a current compliance is enforced during a SET operation; otherwise, the unchecked high current through the device will permanently establish an LRS by electrically breaking down the oxide. Once the device is in the LRS, it may be returned to the HRS via a RESET operation, typically by applying a lower voltage, V_{RESET}, sans the current limit.

Though Chua only explicitly predicted one switching style, four switching styles are observed in practice. When V_{SET} and V_{RESET} are of opposite polarity, the device is said to be bipolar. Furthermore, if V_{SET} = +V, then the device is said to be bipolar(+) (Figure 2.2.1 a)); else if V_{SET} = -V, the device is bipolar(-) (Figure 2.2.1 b)). When V_{SET} and

V_{RESET} are of like polarity, the device is said to be unipolar. After the same fashion, if V_{SET} = +V, then the device is said to be unipolar(+) (Figure 2.2.1 c)); else if V_{SET} = -V, the device is unipolar(-) (Figure 2.2.1 d)). Should a device exhibit both bipolar and unipolar switching, the device is said to be nonpolar. If all four bipolar and unipolar switching configurations are exhibited, the device may be said to be completely nonpolar.

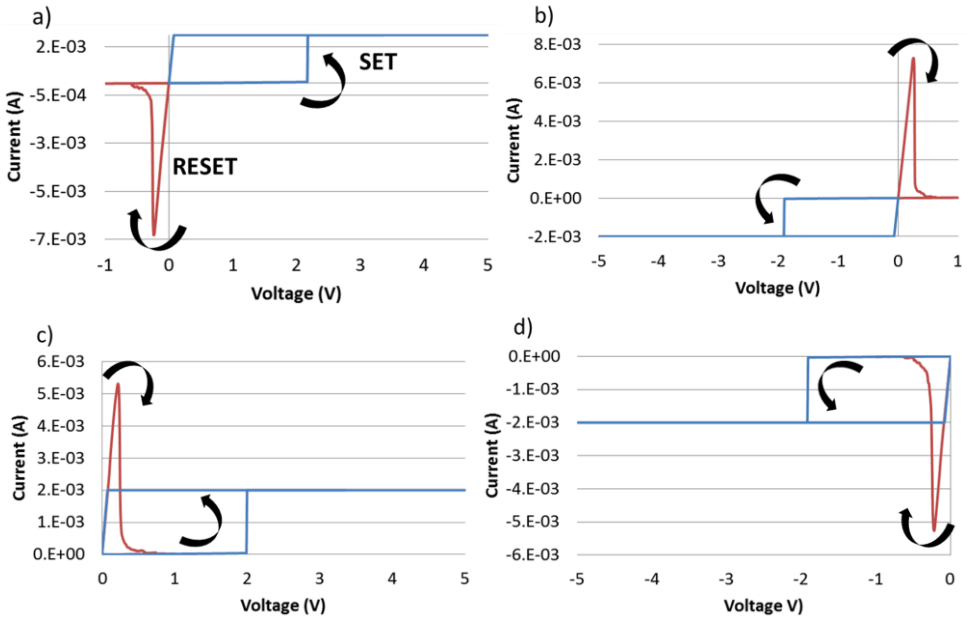


Figure 2.2.1 I-V curves of all four possible switching styles were observed in memristive devices (data from Section 3.4), a) bipolar(+), b) bipolar(-), c) unipolar(+), and d) unipolar(-), where the blue curve is the SET operation and the red curve is the RESET operation

c) Cu_xO Memristive Devices

Copper oxide is not a new material in the study of memristive devices [46-49]. Copper is of interest because of its pervasive use in the semiconductor industry. Additionally, several means to create Cu_xO are available in a CMOS foundry. Like other binary oxides, Cu_xO/Cu memristive devices reported in the literature were often simple MIM

structures, which greatly simplified manufacturability logistics. Lastly, nonpolar behavior was reported in Al/Cu_xO/Cu memristive devices, which allows for a greater variety of potential applications for a viable device [43].

Despite the advantages of copper and its naturally occurring oxide, Cu_xO is a difficult material to consistently manufacture. Several studies have used different means to create Cu_xO layers, including thermal oxidation [50], ion implantation [51], and physical vapor deposition [52]; but devices subsequently fabricated from these layers commonly did not have long endurance times (~10^4 cycles) [48] and suffered from interfacial voiding [52] that limited their wide-spread use. Of the available synthesis techniques, copper oxide created by plasma oxidation (POX) [7] exhibited the most robust switching properties.

Copper oxide manufacturing inconsistencies have led to two reported switching mechanisms: trap state filling/emptying [15] and filament formation/rupture [43]. To properly evaluate Cu_xO memristive devices fabricated under a certain process, the switching mechanism(s) involved ought to be unambiguously identified.

2.3 Application space

The transistor was foundational to the success of the computer revolution. While it is now possible to fabricate billions of transistors onto a single computer chip, the sheer number of transistors consistently increases the operational power requirements and excess thermal energy which must be dissipated. As portable technology becomes

increasingly significant in today's economy, memristive devices successfully integrated with current CMOS technology have the potential to become game changing.

As previously stated, memristors are nonvolatile electrical potentiometers. Furthermore, they may be as simple to fabricate as a MIM structure. In terms of advancing current computing paradigms, memristors will likely be employed to reduce the size, weight, and power (SWaP) requirements of integrated circuits.

Static random-access memory (SRAM) and dynamic random-access memory (DRAM) are two primary means for volatile memory storage used in computers today. These memory cells are composed of transistors which much be periodically refreshed, or the stored bit will be lost. Additionally, by virtue of using transistors, a voltage bias is continually applied to the drain of the transistor.

Given that the memristive device can be programmed and may persist in that state until reprogrammed otherwise, it is expected that memristive devices will be used to replace a significant number of transistors to create a reduction in the overhead power costs. Furthermore, by strategically replacing transistors with memristive devices, not only could integrated circuits be made reconfigurable, but currently reconfigurable circuits could be made non-volatile, e.g. field-programmable gate arrays (FPGA) [53].

Given the simplicity of the MIM structure, it was natural that crossbar arrays were quickly identified as potential architectures for integrating memristive devices with

CMOS [54-57], where the switching layer would be sandwiched between two orthogonal metal lines (Figure 2.2.2). The device area would be only that of the line width squared, so the achievable memory storage density could exceed 1 TB/cm^2 [59]. In theory, each device would be addressable by applying a voltage to the appropriate *x* line and *y* line.

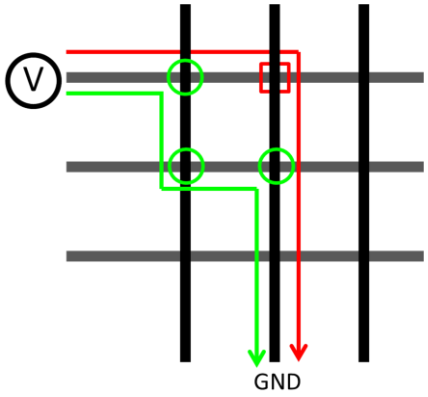


Figure 2.3.1 A crossbar architecture with memristive devices between the metal lines at the intersection points theoretically allowed addressing of individual devices (red square) by applying a voltage to row *x* and electrically grounding column *y* (red path). Sneak paths in crossbar architecture arose because the current followed the path of least resistance (green path), viz. devices already in the LRS (green circle). Thus the measured resistance value could not be trusted to be that of the intended device.

However, in practice, crossbars suffer from two problems: sneak paths and crossbar line resistance limits. While voltage was restricted to the metal lines to which it was applied, the subsequent current flow was not [57] (Figure 2.2.2). Thus, even the success of a WRITE/ERASE (i.e. SET/RESET) operation was unverifiable. It has been proposed that fabricating memristive devices back-to-back or a memristive device and diode in series may be used to counter these sneak paths [57, 60].

Additionally, there were physical limits to the practical size of memristive device crossbars. As the crossbar line length increased, the total resistance of the metal line increased. Even allowing for sneak path mitigation techniques, as the line resistance increased, more of the applied voltage bias was across the line itself and not the memristive device at the crossbar junction [61].

The last feature of the memristive device to be of great promise is the multi-state capability exhibited by some devices. The advantages of more than one bit of information storage per device are self-evident. This property also naturally lends these devices for applications in another, very different computing paradigm.

All of the previously discussed applications of memristors have been restricted to classical or von Neumann computing architectures, where data and instructions are fetched and executed sequentially [62]. Neuromorphic computing, on the other hand, attempts to perform computation in a manner analogous to biological systems. This novel approach recognizes that biological systems perform massively parallel, asynchronous computations using highly interconnected neurons. These neurons are connected by numerous synapses with adjustable weights. It is the adjusting of these synaptic weights that allows a biological system to learn [4]. The SWaP savings and brute computational prowess of this computing paradigm is evident from even as simple a comparison as a dragonfly's aerial maneuvering and landing with that of an F-22 Raptor.

Again the synaptic plasticity is one of the key requirements. In software simulations of neural networks (collections of neurons and synapses), updating the synaptic weights was a straightforward operation. Hardware implementations of synapses were often hybrid hardware/software solutions and required many different circuit elements [63-68]. Hardware synapses on very-large-scale integration (VLSI) chips required a disproportionate amount of real-estate, so it quickly became apparent that such a hardware approach would be not be able to achieve the neuron & synapse counts of relevant biological systems. Even a simple roundworm (*Caenorhabditis elegans*) has 302 neurons and about 5,000 synapses [58], which is trivial compared to the billions of neurons and trillions of synapses in the human brain.

The memristive device is the hardware equivalent of the biological synapse [3, 4]. Not only can its resistance value, the synaptic weight, be modulated ("trained"), but an external power source is not required to maintain this value. Furthermore, this hardware synapse is a single two-terminal device; and, being a MIM, may theoretically may be made on size scales similar to transistors. Neuromorphic learning circuits including memristive devices have already been demonstrated to replicate the learning behavior of an amoeba (*Physarum polychephalum*) [69] and "learned" associative memory (e.g. Pavlov's dog) [70].

Despite all the promises of memristive devices, it is still a maturing technology with respect to commercial applications. First, only certain materials are allowed in the FEOL and in the BEOL of a CMOS foundry; so a manufacturable device must be composed of

only approved materials. Second, switching voltages and resistance values must be consistent across devices. Third, the retention time of a device ought to be comparable to Flash, >10 years. Fourth, the device ought to have an endurance comparable to Flash, 1 million switches.

2.4 Summary

Memristors and their associated behaviors were theoretically predicted back in 1971. Since then numerous memristive devices bearing the signature pinched hysteresis I-V curve have been fabricated, though the actual switching mechanism was dependent upon the materials used. The nonvolatile, variable resistance properties of these devices make them desirable for commercial applications ranging from classical to neuromorphic computing. Today, this technology is still in its infancy; and more basic science as well as device engineering research must be invested before the full impact of the memristive device upon computing can be accurately assessed.

III. Methods & Procedures

3.1 Introduction

This chapter covers the methods and procedures used during the execution of this research. While the general procedures for fabrication and testing were consistent throughout, several parameter values were changed as required. These changes will be detailed in the appropriate subsections of Chapter 4.

3.2 Fabrication

A starting substrate of SiO_2/SiN was fabricated on 300 mm silicon wafers using standard chemical vapor deposition (CVD) techniques. Atop the substrate, Cu/Ta/TaN were deposited by physical vapor deposition (PVD), acting as the electroplating seed, adhesion layer, and diffusion barrier, respectively. To create the bottom electrode, 1µm of electrochemical deposition (ECD) Cu was deposited on the Cu seed layer. Chemical mechanical planarization (CMP) was then used to level and polish the ECD Cu.

Cu_xO films were grown via plasma oxidation (POX), a common process in semiconductor manufacturing because of its low temperature requirements and high oxidation rates. For the first generation of devices, plasma oxidation was performed in the 300 mm facility at the College of Nanoscale Science & Technology, University at Albany, SUNY (CNSE). The plasma oxidation recipe used for the second and third generation Cu_xO films required the use of a different plasma oxidation system, a 200 mm Trion Phantom III RIE (reactive ion etch) system. This system allowed for two power settings: RIE and inductively coupled plasma (ICP) power (Figure 3.2.1). Plasma, which

is ionized gas molecules, was created by a radio frequency electromagnetic field applied at hundreds of watts (ICP power) to the system, where the oscillating field liberated electrons from the gas. The RIE power supplied a DC bias of hundreds of volts to the wafer chuck, which drew the negatively charged gas ions to the wafer. In this manner, the attracted ions either etched the surface of the target wafer or reacted chemically to it. In this case, Cu_xO was grown. Aside from the RIE and ICP power levels, plasma oxidation etch rates/oxide growth were dependent upon a) the wafer chuck temperature, b) the process duration, c) the gas flow rate, and d) the chamber pressure.

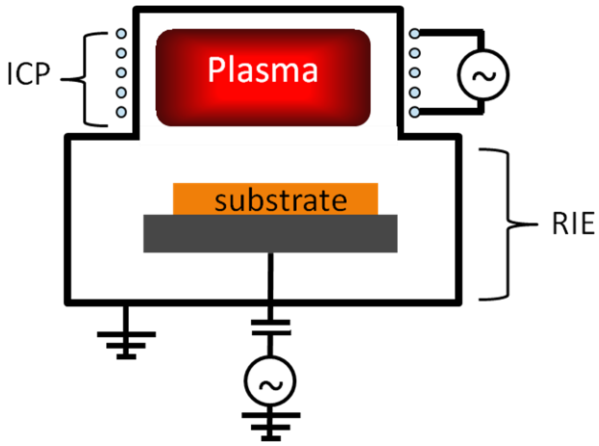
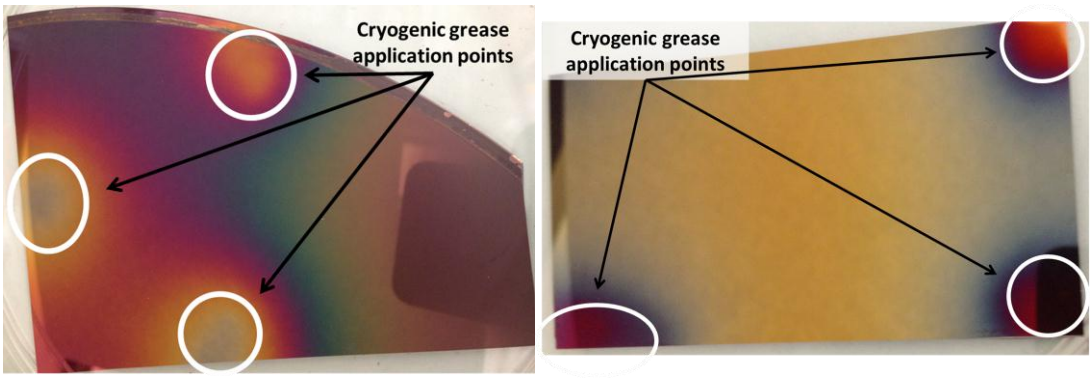


Figure 3.2.1 Figure shows schematic view of a plasma oxidation chamber.

The Trion Phantom III RIE system was designed for 200 mm wafers, thus sections of the Cu wafer had to be cleaved and adhered to an 200 mm Si carrier wafer by means of cryogenic grease. The use of the grease ensured that the smaller sample would not become dislodged during mechanical transport between the loading and oxidation chambers of the tool or during the POX process itself but would be removable after the oxidation process was complete.

The carrier wafer and cryogenic grease had some unintended consequences on the resulting Cu_xO films. The wafer chuck temperature was varied during experimentation. For the last two generations of devices, the chuck temperature was set to 0° C. Since RIE was a thermally sensitive process, the areas with a liberal application of cryogenic grease were held closer to the programmed chuck temperature than the surrounding areas. At the end of the oxidation step, these areas remained close to the coloration of the native oxidation layer of Cu. Moving away from these points, a color gradient was observed (Figure 3.2.2). The effects of the cryogenic grease placement were confirmed by varying the points of grease application and observing corresponding positions of the points of minimally oxidized Cu coloration (Figure 3.2.2 a) & b)).

Since the colors did not change with the angle of incidence (Figure 3.2.3), the color gradient resulted from physical differences in the Cu_xO itself, e.g. the oxide thickness [100]. For data analysis continuity, all reported device data were collected from devices populating the most uniformly colored regions beyond the cryogenic grease application points. Since temperature was not an explicitly tested variable during this research, a consistent temperature was more important than the absolute temperature value itself.



a) b)

Figure 3.2.2 Cryogenic grease was applied to the backside of the areas inside the white circles of a) RIE 300 W sample and b) RIE 200 W sample. The areas of least color deviation from the control Cu wafer corresponded to the areas of cryogenic grease application across all samples. The color gradient of a) is more expansive because the grease was spread out farther on that sample than in sample b). The surface of both samples were still highly reflective but were diminished in the picture for maximum color contrast. (The dark shadow on the right side of a) is the camera.)

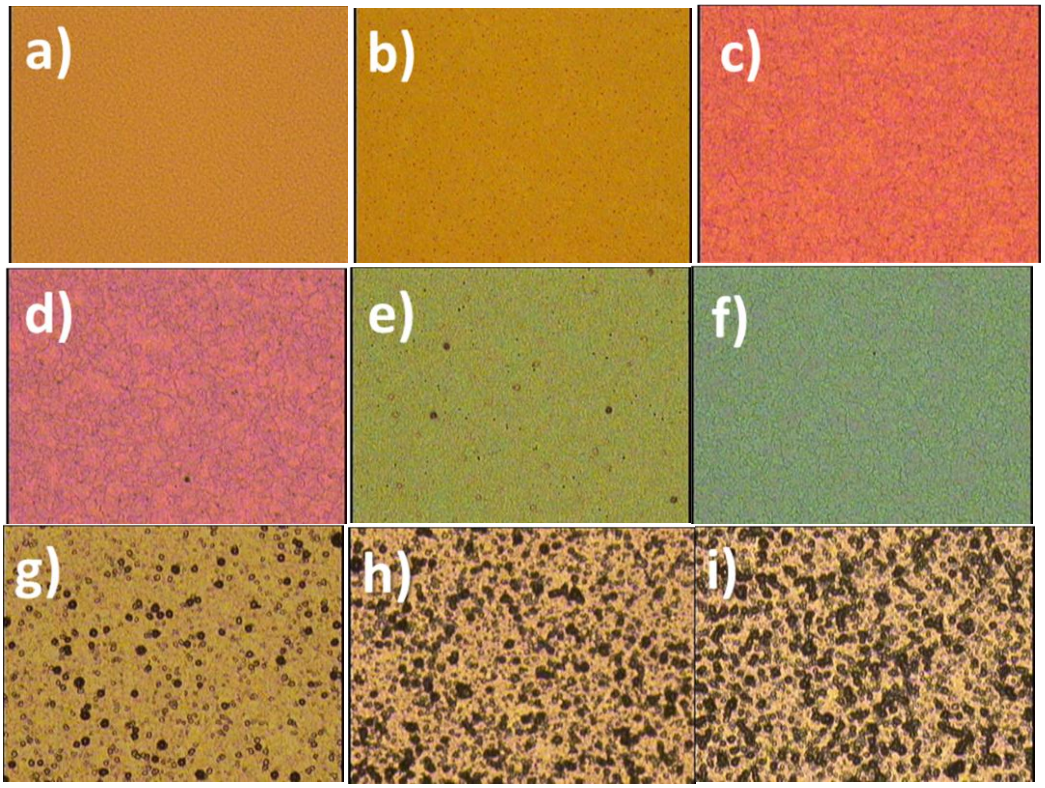


Figure 3.2.3 a) Cu wafer sample arrived with native oxide layer and uniform coloration. Following the plasma oxidation step, a variety of colors of Cu_xO were observed, b) yellow, c) orange, d) purple, e) light green, f) green, and g) brown 1, h) brown 2, and i) brown 3. Pictures b) – i) taken from RIE 300 W sample from Section 4.4.

Furthermore, as is discussed later, the bare Si carrier wafer was a likely source of the Si contamination observed in the oxide. To mitigate this potential contamination source, a Cu coated carrier wafer was procured for the third fabrication runs. Those oxide films did not have significant Si concentrations as before.

Next, top electrodes (TE) were either patterned using a custom photolithography process for 200 mm CMOS technology or a shadow mask. For the "standard" photolithography process used in this research, the samples were spincoated with Shipley 1813 resist, heat

treated, and patterned using a contact aligner. The mask set used varied over the course of experimentation and is detailed in the appropriate subsections of Chapter 4. For reference, Figure 3.2.4 is the template for the shadow mask used for devices fabricated in Section 4.4. The TE size of the first four rows are 100 x 100 μm and decrease by 10 μm for each subsequent row down to 10x10 μm. Al TE 200-400 nm thick were deposited via electron beam deposition. For devices defined by photolithography, a separate liftoff step was required to remove the excess Al. Thus the final memristive devices were Al/Cu_xO/Cu material stacks, where the Cu_xO and Cu layers were in common among all devices.

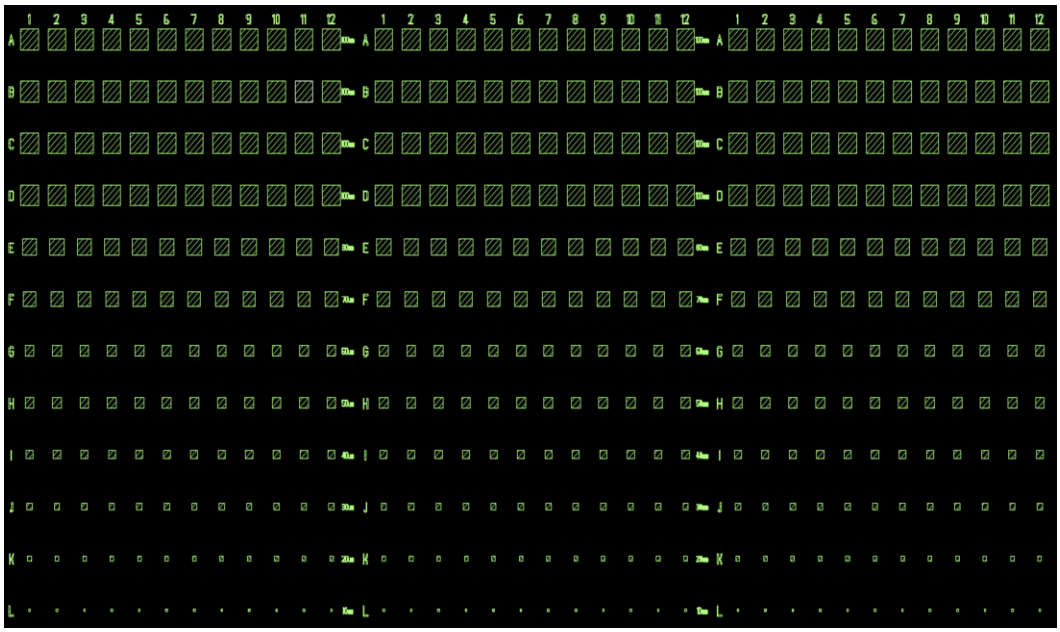


Figure 3.2.4 A variable TE mask pattern was used for the third generation memristive device run. TE sizes range from 100x100 μm to 10x10 μm.

3.3 Characterization

Following the plasma oxidation step, the Cu_xO layer properties were measured. The final copper oxide thickness of each sample was approximated by secondary ion mass spectrometry (SIMS). X-ray photoelectron spectroscopy (XPS) was used to determine the oxygen concentration in the aforesaid oxides.

The completed memristive devices were electrically characterized using a Cascade M-150 probe station and an Agilent B1500A Semiconductor Device Analyzer (Figure 3.3.1). The exact testing parameters varied with the device generation, however, the method of testing remained consistent. Unless explicitly stated otherwise, devices were operated with the voltage bias applied to the Al TE and an exposed Cu bottom electrode (BE) electrically grounded (Figure 3.3.2). For both SET & RESET operations, either "single sweep" or "dual sweep" measurements were taken. In single sweep-mode, the applied voltage sweep progressed from 0 V to ±V in ±10 mV steps. In dual sweep-mode, the applied voltage sweep progressed from 0 V to ±V then back to 0 V in ±10 mV steps. The time between each measurement was not specifiable and was measured to be between 0.04-0.05 s. Lastly, during the SET operation only, a current compliance between |0.5 – 10| mA was enforced to prevent a device from shorting during the transition from a HRS to LRS.

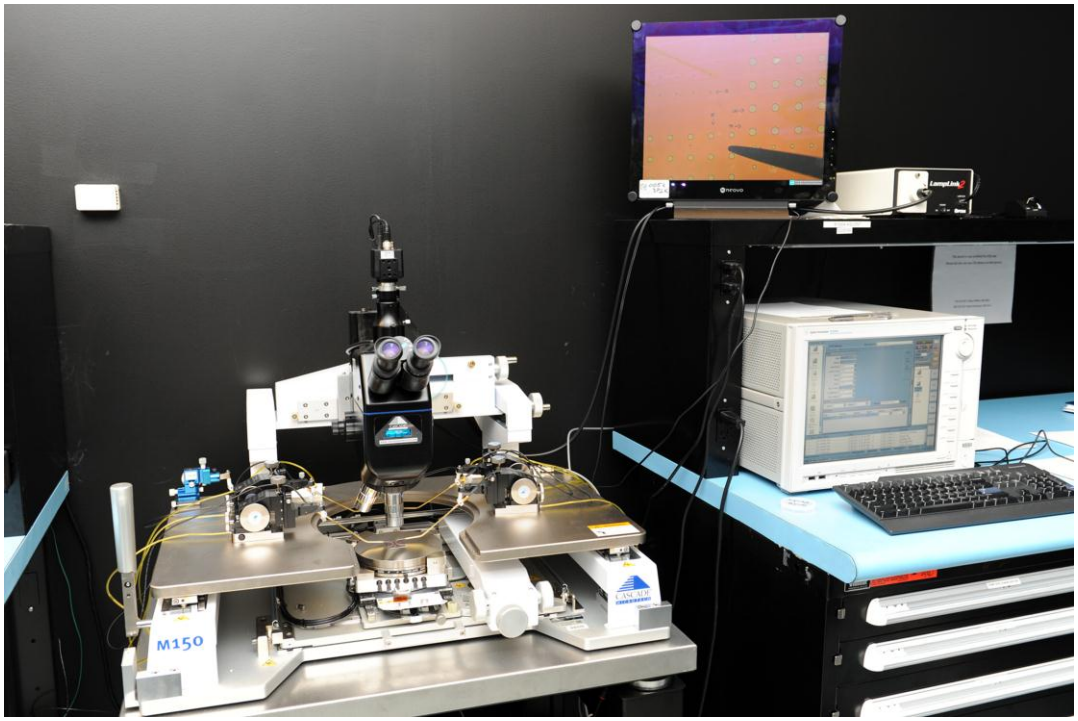


Figure 3.3.1 A probe station (left) and analyzer setup (right) were used for device characterization.

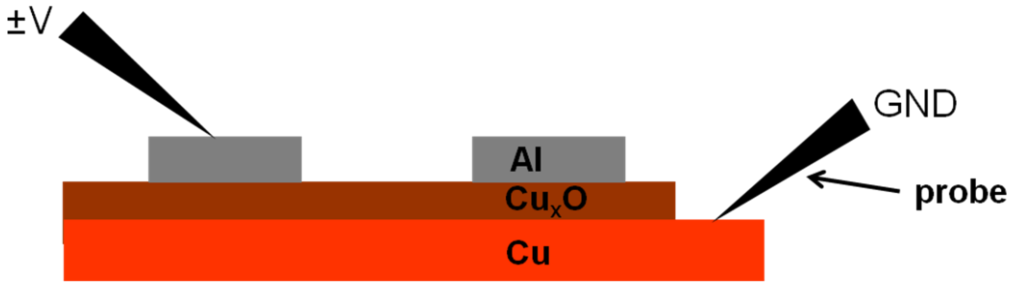


Figure 3.3.2 Figure shows the typical device measurement probe and electrical bias arrangement.

3.4 Modeling

With respect to modeling, several ideal memristor models are presently listed in the literature [3, 72, 73]. These were implemented into MATLAB, and two were

implemented in Verilog-A as well. When these proved inadequate to replicate all the observed device behaviors, piece-wise linear bipolar, unipolar, and nonpolar models were developed by the author. These models were strictly empirical and designed for circuit simulation and not for elucidating physical phenomena.

3.5 Summary

Plasma oxidation was used to grow Cu_xO atop a Cu wafer. Al TE were then defined via photolithography or a shadow mask and deposited via electron beam deposition. The finished devices were electrically characterized via voltage sweeps. Several device models were then created and fit to the experimental data.

IV. Physical Device Experiments

4.1 Introduction

The focus of this research was to determine what oxide physical parameters drastically affected Al/Cu_xO/Cu switching behavior and to identify the switching mechanism employed by these devices. This research was broken into three generations of devices. The first generation involved a wide range of parameter values for the plasma oxidation step that created a baseline understanding. The defects noted in the first generation led to experiments expanding upon a plasma oxidation process in the literature for the second generation [7]. The third generation samples used the same processing conditions as the second generation but with an additional contamination control measure in place, which resulted in improved device performance.

Throughout the literature of Cu_xO/Cu memristive devices, the switching mechanism has been attributed to several different physical phenomena [7, 44, 46]. While these conflicting conclusions may correctly reflect the variations of the respective fabricated oxide thin films, they proved insufficient to account for all the behaviors observed in the thin films fabricated for this research. Thus a device specific switching mechanism theory is herein proposed.

4.2 First Generation Cu_xO Growth Techniques

a) Oxide Growth & Device Fabrication

Since Cu_xO is a naturally occurring oxide, it was necessary to develop a general understanding of the sensitivity of Cu thin films to the plasma oxidation processing

conditions. A range of times, power levels, and O_2 flow rates were used while maintaining a constant pressure of 500 mT at 30° C (Table 4.2.1). The resulting film thicknesses were measured via transmission electron microscopy (TEM) (Figure 4.2.1). While the processing conditions ranged significantly, the resulting oxide layers were all extremely thin (< 10 nm) and crystalline to varying degrees as indicated by the parallel lines in the oxide layer.

Table 4.2.1 First generation Cu_xO thin film plasma oxidation conditions

Name	Time (min)	Power (W)	O_2 Flow Rate (sccm)	Temperature (° C)	Pressure (mT)	Substrate
POX-10	10	500	1000	30	500	ECD Cu
POX-11	10	1000	1000	30	500	ECD Cu
POX-12	20	300	14000	30	500	ECD Cu
POX-13	30	300	14000	30	500	ECD Cu

A standard lithographic process was used to define circular top electrodes of varying sizes, viz. 25, 50, 75, and 100 µm diameter. Al TE 100 nm thick were deposited via electron beam deposition. A liftoff process was then used to remove the excess Al from the wafer leaving discrete TE (Figure 4.2.2).

b) Device Characterization

The memristive devices were characterized using a probe station and parameter analyzer as described in Chapter 3. Devices were cycled between the HRS and LRS (one SET & one RESET operation) in single sweep-mode. The voltage bias was applied to the Al TE, and an exposed Cu BE was electrically grounded.

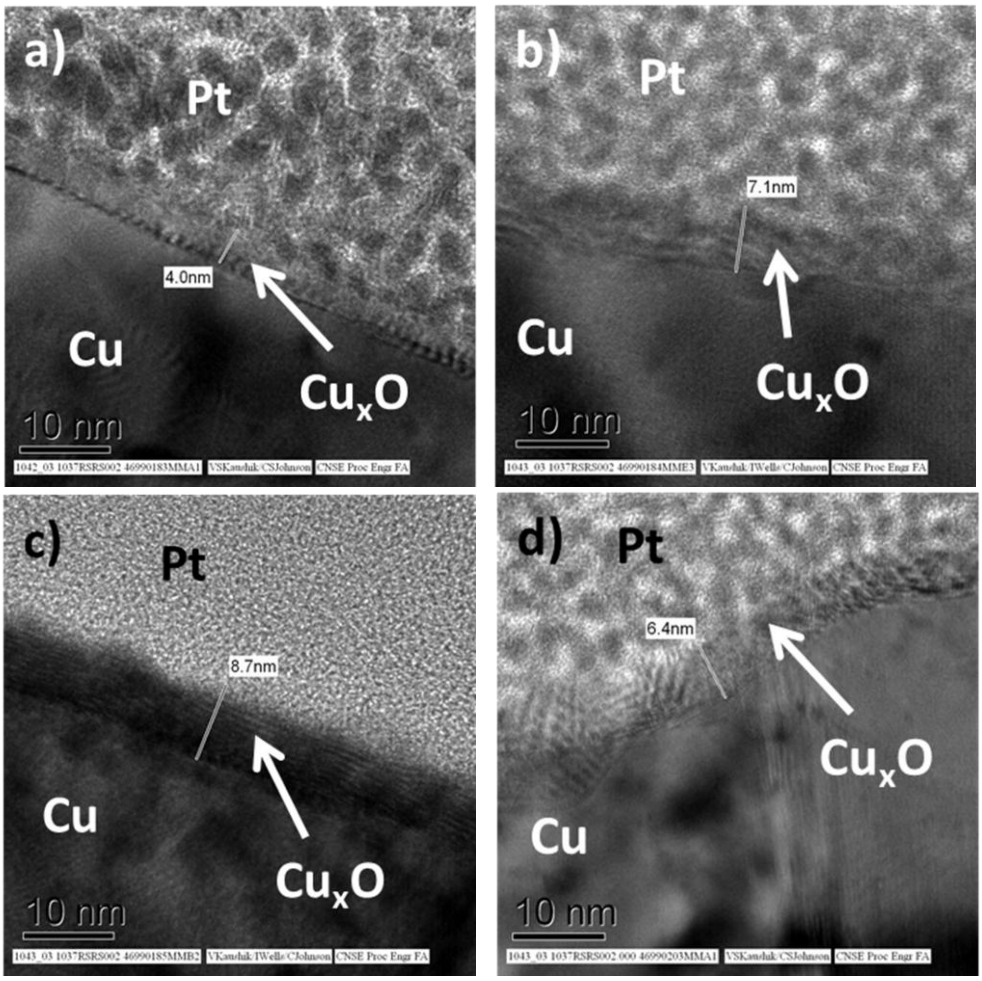


Figure 4.2.1 Despite large variations in processing parameters, TEM images of resulting Cu_xO layer thicknesses indicated extremely thin oxides of varying degrees of crystallinity, a) POX-10, ~4 nm; b) POX-11, ~7 nm; c) POX-12, ~7-9 nm; and d) POX-13, ~6 nm. A platinum protective layer was deposited over the oxide prior to imaging. (Images courtesy of V. S. Kaushik and C. S. Johnson (upper left and lower right) & V. Kaushlik, I. Wells, and C. Johnson (upper right and lower left).)

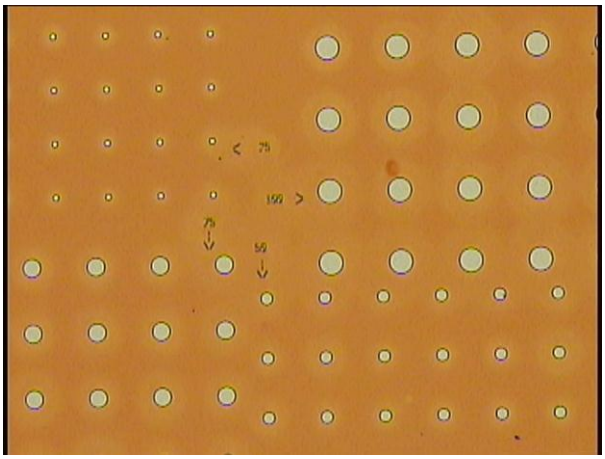


Figure 4.2.2 This picture shows a field of memristive devices of varying TE size, 25 µm (upper left), 50 µm (lower right), 75 µm (lower left), and 100 µm (upper right).

The yield of viable devices across all four samples was low, 10 - 15%. Devices on all four samples which did switch demonstrated very inconsistent SET/RESET curves, though POX-10 and 11 devices had the most consistent I-V curves of the lot. The devices collectively demonstrated complete nonpolar behavior, though bipolar(+) (Figure 4.2.3 a)) and unipolar(+) (Figure 4.2.3 b)) were predominately demonstrated. No forming step was required outside of the typical operating voltages. V_{SET} ranged from |0.8 – 5| V, and V_{RESET} ranged from |0.2 – 1.8| V. Devices tended to spontaneously RESET faster when the current compliance was below 25 mA. Thus, their memory function was limited. The HRS resistance varied greatly in the mega-ohm and giga-ohm range, and the LRS resistance ranged between 4 - 60 Ω. Due to the inconsistency of the switching behavior, there was no discernible behavioral dependency upon contact size.

Aside from the irregularity of the SET and RESET curves, the chief defect in the device operation was the short LRS retention time. Once SET, the devices typically persisted in an LRS for about 10 s, though some devices remained SET for up to 15 min. Again,

increasing the current compliance during a SET operation prolonged the LRS retention time; but this was not a viable solution to the problem.

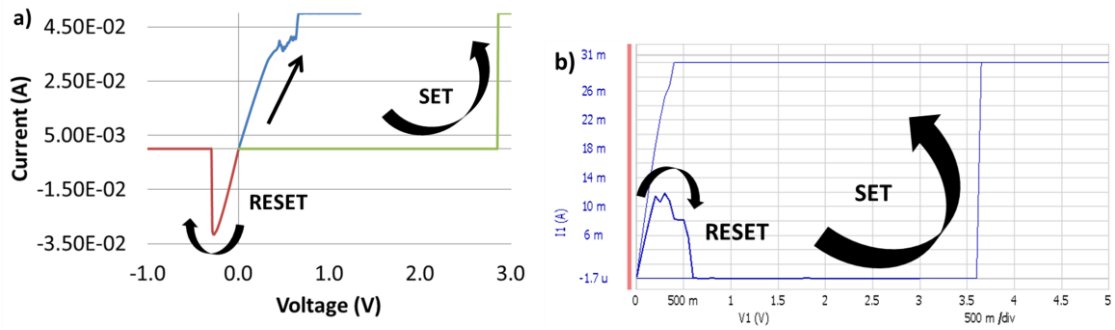


Figure 4.2.3 The figure a) depicts a bipolar(+) switch of a POX-12 memristive device, and figure b) depicts a unipolar(+) switch of a POX-10 memristive device.

At first glance, this low retention time might be attributed to the thickness of the copper oxide layer alone. Memristive devices had previously been reported with 12 nm of thermally grown copper oxide [6] without mention of low memory retention rates. In retrospect, suboptimal device behavior was attributed to the standard photolithography process (Section 4.3 *b)*). Thus all the sources of inconsistent device switching behavior could not be isolated in this data.

c) Further Oxide Growth Experiments

Since the minimum reported thickness in Cu_xO resistive memory literature is 12 nm, it was thought that a thicker oxide was potentially required for consistent device switching. In this trial, four wafers with 1 µm of ECD Cu and two wafers of 1 µm of PVD Cu were prepared according to Table 4.2.2, where ECD Cu wafer Slot 4 served as a control wafer

to account for native oxide growth. The resulting copper oxide statistics are detailed in Table 4.2.3.

Table 4.2.2 Second set of first generation Cu_xO thin film plasma oxidation conditions

Substrate	Slot	Time (min)	RF Power (W)	O_2 Flow Rate (sccm)	Temperature (° C)	Pressure (mT)
ECD Cu	1	30	300	1000	280	2500
ECD Cu	2	30	1000	1000	280	2500
ECD Cu	3	30	0	14000	280	2500
ECD Cu	4	-	-	-	-	-
PVD Cu	1	30	0	14000	280	2500
PVD Cu	2	30	300	1000	280	2500

Table 4.2.3 Approximate copper oxide film thickness values

Substrate	Slot	Cu_xO thickness (nm)	Cu substrate thickness (nm)
ECD Cu	1	169-172	838
ECD Cu	2	746	461
ECD Cu	3	139-167	812
ECD Cu	4	-	-
PVD Cu	1	815	471
PVD Cu	2	738	568

The most important result from this set of wafers was the significant voiding at the Cu_xO/Cu interface observed across all samples (Figure 4.2.4), save the control wafer. The degree of voiding observed precluded any attempt at successful device fabrication. Despite the fact that copper readily oxidizes, the most significant result from this trial was the demonstration that the controlled growth of high quality Cu_xO was not a trivial endeavor.

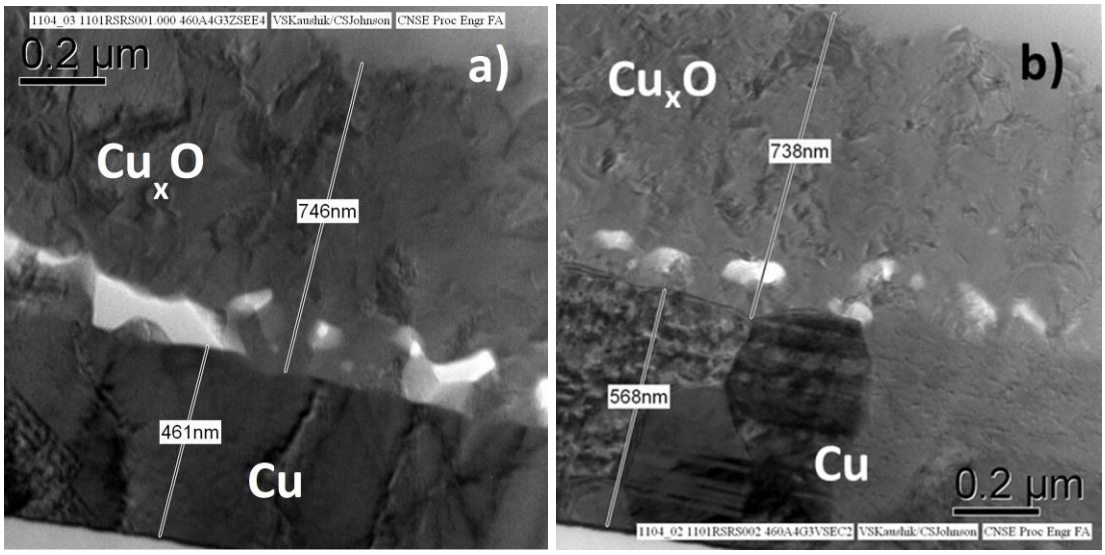


Figure 4.2.4 Significant voiding at the Cu_xO/Cu interface from the plasma oxidation process as seen in a) ECD wafer Slot 2 and b) PVD wafer Slot 2

4.3 Second Generation Cu_xO Growth Technique

a) Oxide Growth & Device Fabrication

Instead of independently deriving a working plasma oxidation recipe, the recipe described by Lv, *et al.* [7] was adopted. This recipe was modified to study the effects of the plasma oxidation parameters on device switching behaviors. Three 1 μm ECD Cu coated wafer samples were prepared for 10 min under 10 sccm O_2 at 45mT, the RIE power was varied from 100-300 W, and the ICP was fixed at 300 W (Table 4.3.1). A standard photolithographic process was used to define the TE.

Table 4.3.1 Second generation Cu_xO thin film plasma oxidation conditions

Name	Time (min)	RF Power (W)	ICP Power (W)	O_2 Flow Rate (sccm)	Temperature (° C)	Pressure (mT)
POX-20	10	300	300	10	0	45
POX-21	10	200	300	10	0	45
POX-22	10	100	300	10	0	45

Although 400 nm of Al was to be deposited via electron beam deposition onto each wafer sample, the high voltage gun malfunctioned during the deposition process. Only 75 nm of Al were deposited by this time, but since it was thought that the thickness of the TE would have no electrical impact upon the memristive devices, they were characterized as fabricated. In most cases, the Al TE proved too thin to adequately prevent the probe from scratching through it and shorting the device. However, for some of the devices tested, switching behavior was observed (Figure 4.3.1). This was sufficient evidence of fabrication success to perform a second 400 nm Al TE deposition run on remaining pieces of POX-20 - 22 wafers. In a moment of at least scientific serendipity, due to time constraints, a shadow mask was used to define the Al TE (195 µ diameter) instead of the typical photolithography process.

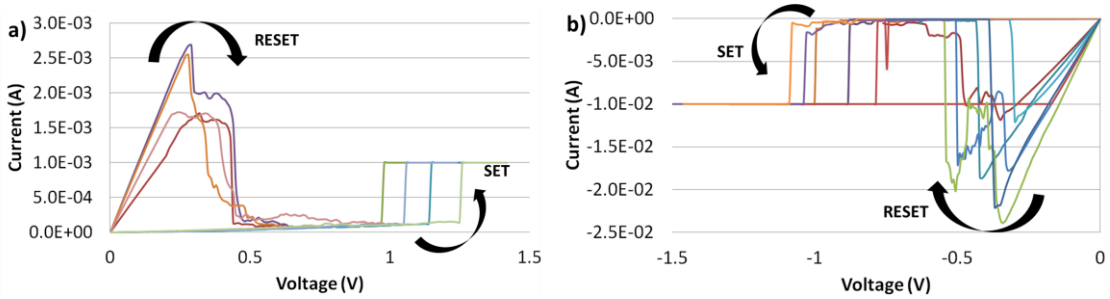


Figure 4.3.1 While the I-V curves were not very consistent, POX-22 memristive device clearly demonstrated a) unipolar(+) (4 cycles) and b) unipolar(-) (5 cycles) switching.

SIMS was used to determine the material cross-section of the material stack. X-ray photoelectron spectroscopy XPS was used to determine the oxygen concentration in the aforesaid oxides. Between the two measurements the oxide thickness was approximated

(Table 4.3.2). Cupric oxide, CuO, formed on the RIE 100 W sample; and on the RIE 300 W sample, the film was closer in stoichiometry to cuprous oxide, Cu_2O. While the oxide thickness did not monotonically increase with the RIE power, the oxygen concentration generally decreased with RIE power. Due to the nature of the oxide growth method and the non-stoichiometric nature of the RIE 200 and 300 samples, a non-negligible number of positively charged oxygen vacancies are expected in these samples [71]. As a result of the point defects, it followed that the RIE 200 W and 300 W Cu_xO films were expected to be *p*-type semiconductors [5]. The influence of these defects on the switching properties will be discussed in Section 4.5 *b)*.

Table 4.3.2 Copper oxide thicknesses and Cu:O concentrations

Name	ICP power (W)	RIE power (W)	Oxide thickness (nm)	Cu:O (atm.%)
POX-22	300	100	42	50:50
POX-21	300	200	618	55:45
POX-20	300	300	488	60:40

Unexpectedly, XPS analysis showed that a non-negligible amount of Si was present in the Cu_xO/Cu following the plasma oxidation step (Figure 4.3.2). Thermal drive-in from the underlying Si wafer into the initial copper film was ruled out considering the TaN barrier layer beneath Cu/Ta layers. A more probable source of contamination was the use of the Si carrier wafer during the plasma oxidation step (Section 3.2). It was hypothesized that during the plasma oxidation, Si atoms were displaced from the carrier wafer and redeposited onto the Cu sample. The effectiveness of the contamination countermeasures (Section 3.2) supported this conclusion.

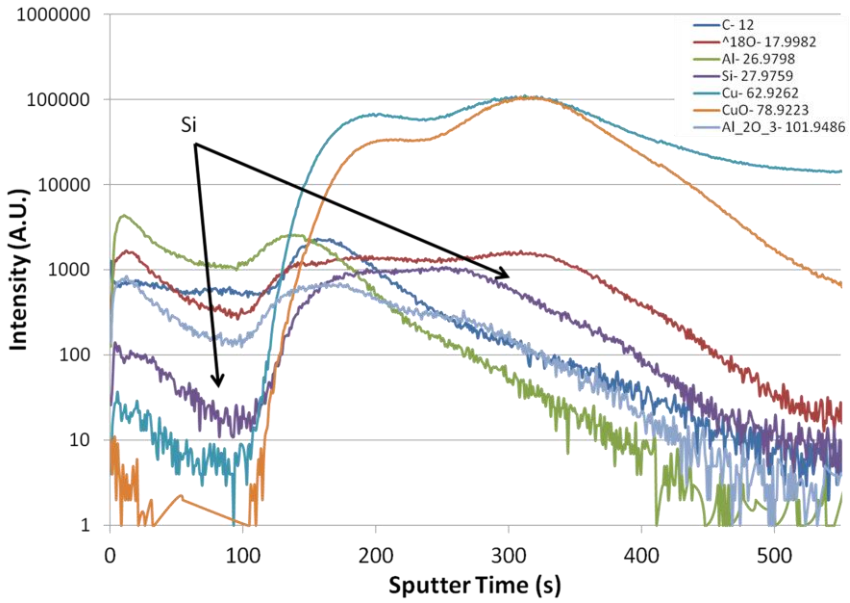


Figure 4.3.2 SIMS plot of material found in POX-22 device indicated Si as a contaminant

b) Device Characterization

Characterization of the memristive devices was performed using dual sweep-mode voltage measurements. For all reported measurements, the Al TE was biased and an exposed Cu BE was grounded.

Memristive devices from all three samples exhibited stable, complete nonpolar switching behaviors over repeated SET/RESET measurements (Figure 4.3.3). For each sample, devices were manually cycled 20 - 40 times (4-5x per switching style). The I-V curves were significantly more consistent for these shadow masked devices (Figure 4.3.4) than the photolithography devices (Figure 4.3.1) though they were created from the same Cu_xO/Cu wafers (POX-20 – 22). A current compliance between |1-5| mA was required to limit the current during the SET process and ultimately prevent the devices from

undergoing breakdown. SET currents below this range resulted in unstable switching behavior. In general, an initial forming step outside of normal operating parameters was not required unless a non-linear I-V curve was observed in the HRS (Figure 4.3.3 c)). This non-linear I-V behavior is discussed in more detail in Section 4.5 *b)*.

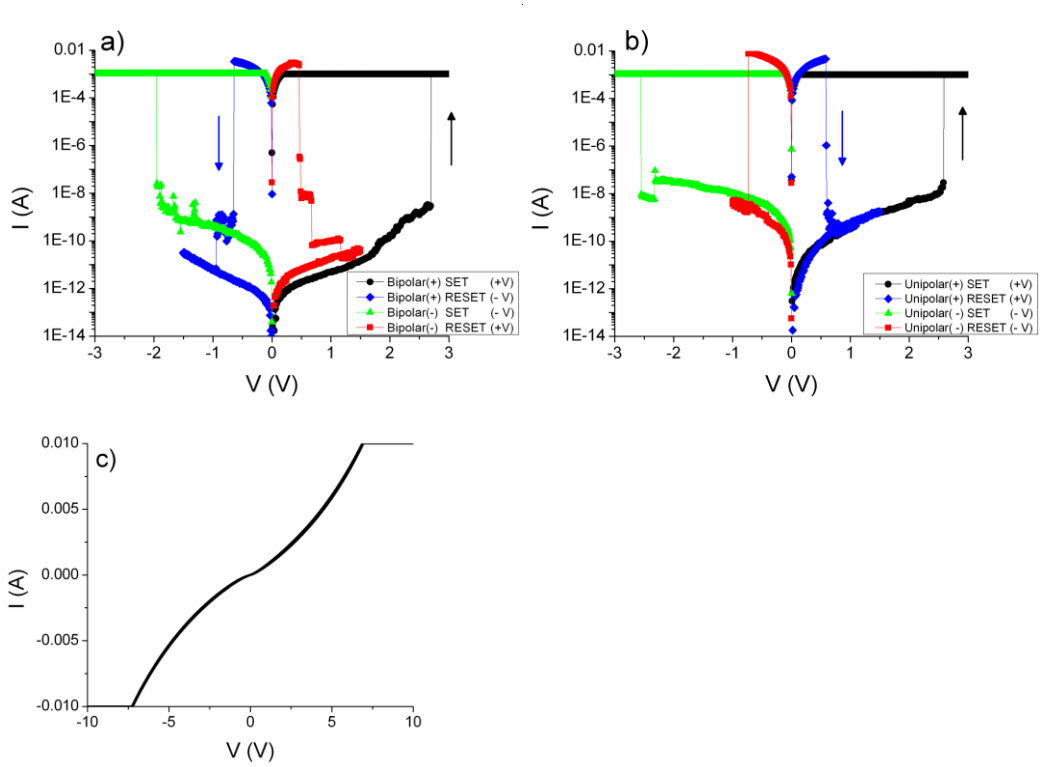


Figure 4.3.3 Complete nonpolar switching was exhibited by second generation Al/Cu_xO/Cu memristive devices. a) depicts typical bipolar switching behavior associated with both positive and negative device bias from RIE 300 W sample, e.g. a bipolar(+) cycle was achieved when a device was SET by a +V sweep (black arrow) and subsequently RESET by a -V sweep (blue arrow). b) depicts typical unipolar switching behavior associated with both positive and negative device bias for the same device tested in a), e.g. a unipolar(-) cycle was achieved when a device was SET by a -V sweep (black arrow) and subsequently RESET by a -V sweep (blue arrow). c) depicts non-linear, non-switching memristive device from RIE 100 W sample.

The operating parameters of these nonpolar devices are listed in Table 4.3.3. It is evident that neither the V_{SET} nor V_{RESET} values trended with either the oxide thickness or oxygen concentration. Furthermore, the switching voltages, V_{SET} and V_{RESET}, were consistent and independent of the switching style and polarity. The HRS resistance in the RIE 100 W sample varied by up to an order of magnitude from 40 kΩ. In the other two samples, the HRS resistances consistently ranged from 2 - 3.5 kΩ. Across samples, the LRS resistance was consistently <100 Ω.

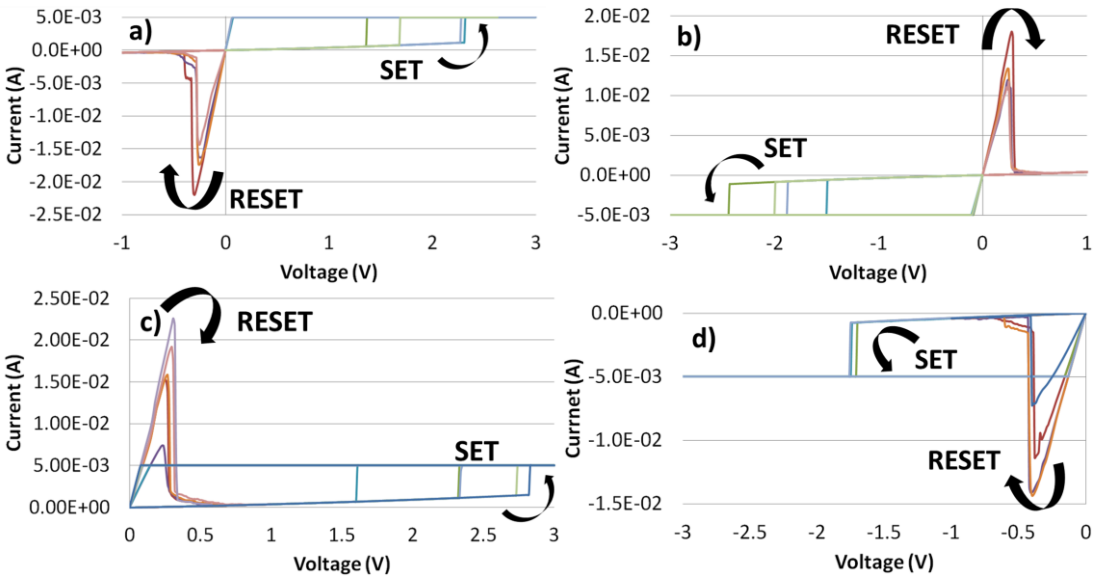


Figure 4.3.4 Complete nonpolar behavior over 4-5x cycles per switching style demonstrated on the same device from the RIE 300 W sample, a) bipolar(+), b) bipolar(-), c) unipolar(+), and d) unipolar(-).

Table 4.3.3 Typical operative parameters for second generation memristive devices

Name	RIE Power (W)	|VSET| (V)	|VRESET| (V)	HRS resistance (kΩ)	LRS resistance (Ω)
POX-22	100	2.5-3.0	0.3-0.7	40 – 400	10-100
POX-21	200	2.0-5.0	0.3-0.6	1.85 - 2	15-25
POX-20	300	1.5-2.5	0.3-0.7	3.3 - 3.5	10-15

The nonpolar memristive device yield overall was low, about 10%. For devices that did not switch, a non-linear I-V curve generally symmetric about the origin was routinely observed (Figure 4.3.3 c)). This non-linear behavior was significant for two reasons. 1) These devices could occasionally be switched at high negative voltages, (-5) – (-10) V, with high current compliance values (>|10| mA). However, the subsequent switching voltages of these devices were not consistent; and the devices frequently stopped switching after a small number of SET/RESET cycles (typically <5). 2) When a typical nonpolar device failed (stopped switching), it exhibited a similar non-linear I-V behavior to the devices that did not switch, rather than resorting to the clearly defined HRS or LRS.

To observe the effect of TE size on device switching, TE were patterned (Figure 3.2.4) on another piece of POX-22 wafer using the standard photolithography method. However, comparable devices were not produced using this method. Any devices that did SET spontaneously RESET within seconds.

Since the photolithography process was the sole process variation between these device sets, to identify the exact step responsible for device failure, three samples from the same RIE 300 W wafer were each subjected to one of the photolithography steps. Specifically, in the resist step, Shipley 1813 resist was applied to the first sample. During the baking step, the second sample was subjected to 110° C for 5 min and 90° C for 1 min. The final sample was exposed to 365 nm UV light for 12 sec. 200 nm thick Al TE (195 μm diameter) were deposited through a shadow mask via e-beam deposition.

The samples exposed to the heating step and the UV step exhibited resistive switching similar to the previously described shadow masked devices above. The sample subjected to the resist did not demonstrate switching. This indicated that the application of the photoresist and the adhesion layers negatively affected the device switching behavior. This detrimental effect resulted from either poor electrical contact between the Al and Cu_xO layer due to inadequate cleaning or a chemical reaction between the resist and one of the materials in the film stack. Since this photolithography process was also used during the Section 4.2 research to pattern the TE, it is probable that this step significantly contributed to the poor device performance.

4.4 Third Generation Cu_xO Growth Technique

a) Oxide Growth & Device Fabrication

While the aforementioned devices were operationally satisfactory, the unanticipated Si contaminant needed to be accounted for. Again, the plasma oxidation tool was designed for 200 mm wafers and the supplied Cu coated wafers were 300 mm. Therefore, a carrier

wafer was required to run a sample. Hypothetically, Si from the Si carrier wafer could transfer to the Cu sample during the plasma oxidation step. To prevent this material contamination, an 200 mm ECD Cu coated Si wafer was used as the carrier wafer. By this means, any Cu that was removed from the carrier wafer surface could be inconsequentially redeposited upon the sample surface. Three samples were thus prepared according to Table 4.3.2. Following the plasma oxidation step, 200 nm Al TE were patterned via e-beam evaporation using a shadow mask, as shown in Figure 3.2.4.

Depth and concentration profiles were performed on the bare Cu_xO before the Al TE were deposited (Table 4.4.1). Depth profiles of the oxide layers were performed by SIMS. At the time of writing, the XPS tool was nonoperational, so Auger electron spectroscopy was used to determine the material concentrations.

Table 4.4.1 Copper oxide thicknesses and Cu:O concentrations

Name	RIE power (W)	Oxide thickness (nm)	Cu:O (atm.%)
POX-42	100	70	55:45
POX-43	200	85	53:47
POX-44	300	245	52:48

No significant Si was observed in either sample by either the SIMS or the Auger spectroscopy (Figure 4.4.1). Chlorine was found in all three samples using SIMS. However, the Auger spectroscopy detected Cl in only the 100 and 300 W samples and detected fluorine in the 200 W sample. In this case, the SIMS analysis was judged to be more accurate than the Auger spectroscopy analysis. Furthermore, in the 100 W sample,

the Cl was confined to the surface; but it was present throughout the oxide of the 300 W sample. The high degree of surface roughness may account for the perceived permeation of the Cl species in the 300 W sample.

Both Cl is commonly used during electrochemical deposition of Cu, but such contamination was not observed in the previous 300 mm ECD Cu wafers. Thus, the additional Cl may have been introduced into the system via the Cu coated carrier wafer, which was prepared at a different facility than the sample wafers. These elements may also have been introduced due to the improper cleaning of the plasma chamber after its previous use.

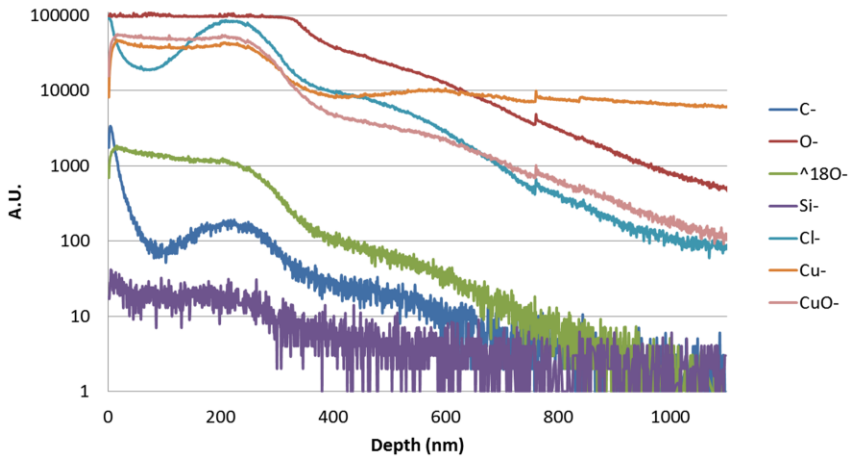


Figure 4.4.1 SIMS plot of material found in RIE 300 W sample. While the Si contamination has been prevented, Cl was detected.

The Cu:O ratios of each film were very close to 1:1 according to the Auger spectroscopy. The measurement error of this technique was around ±10% at. %, which was comparable

to the expected concentration variations between the three samples. These results then only generally support fabrication consistencies with films gown in Section 4.3.

b) Device Characterization

Characterization of the memristive devices was performed using dual sweep-mode voltage measurements. For all of the reported measurements, the Al TE was biased; and an exposed Cu BE was grounded.

Memristive devices across all three samples demonstrated complete nonpolar switching over repeated SET/RESET measurements (Figure 4.4.2). Unlike the devices from Section 3.3, a separate forming voltage sweep, V_{FORM}, between |6.5 – 10| V was required for the RIE 100 W and 300 W samples. Overall, the nonpolar memristive device yield was practically 100%, where improper probing was the identified cause of all initially shorted devices. Devices were manually tested for 20-40 cycles each (4-5x per switching style), often demonstrating very consistent I-V switching curves (Figure 4.4.3). Of particular note, RESETs occurred over a narrow voltage range, $\Delta V \sim 0.5V$, and not over a similar current range. This strongly suggested a voltage driven RESET mechanism.

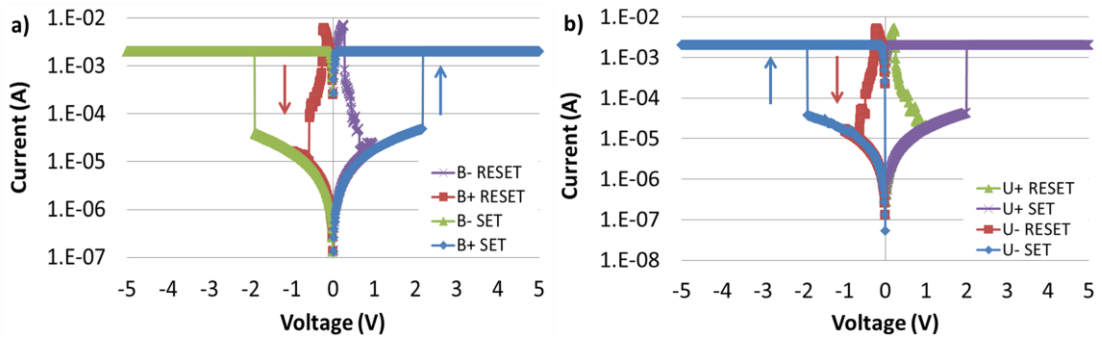


Figure 4.4.2 Complete nonpolar switching was exhibited by third generation Al/Cu_xO/Cu memristive devices. a) depicts typical bipolar switching behavior associated with both positive and negative device bias from RIE 300 W 70x70 μm TE device, e.g. a bipolar(+) cycle was achieved when a device was SET by a +V sweep (blue arrow) and subsequently RESET by a -V sweep (red arrow). b) depicts typical unipolar switching behavior associated with both positive and negative device bias for the same device tested in a), e.g. a unipolar(-) cycle was achieved when a device was SET by a -V sweep (blue arrow) and subsequently RESET by a -V sweep (red arrow).

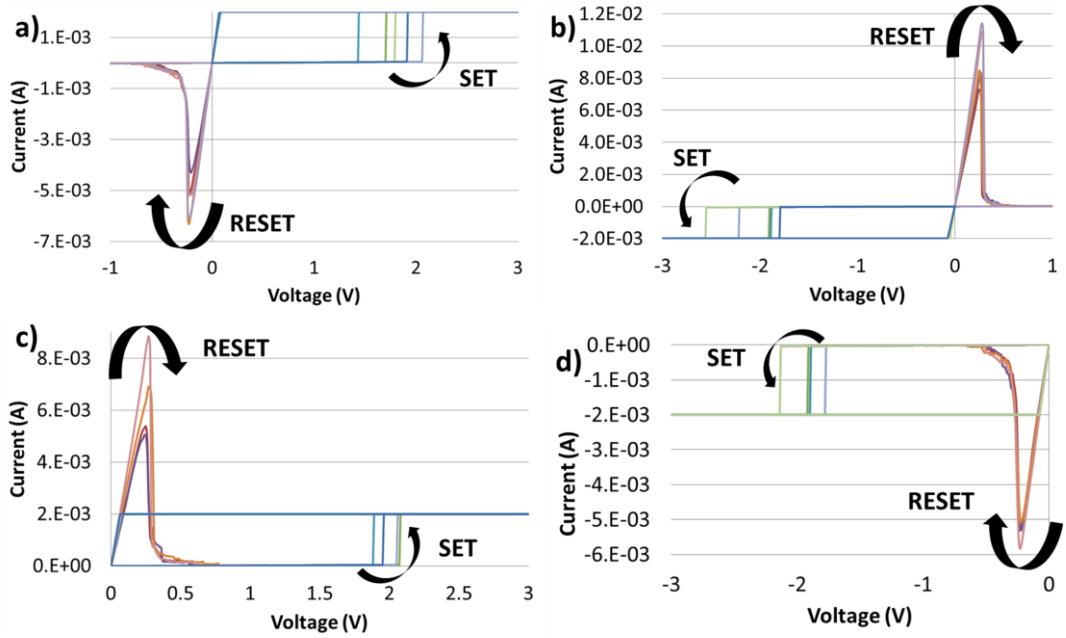


Figure 4.4.3 Complete nonpolar behavior over 4-5x cycles per switching style demonstrated on the same 70x70 μm TE device from the RIE 300 W sample, a) bipolar(+), b) bipolar(-), c) unipolar(+), and d) unipolar(-).

The effects of this initial forming voltage were nonuniform across the RIE 100 and 300 W samples. Forming voltages of |5 – 10| V with |5 – 10| mA current compliances were applied to two devices per TE size from 10 - 100 μm square to identify any forming preferences. One device was subjected to a bipolar(+) then bipolar(-) switch; the other device was subjected to a bipolar(-) then bipolar(+) switch. For devices from the RIE 100 & RIE 300 W samples, a frequent occurrence was a "soft SET," where the device reached the current compliance limit before switching but would be SET by the end of the return sweep. Devices from the RIE 200 W sample would switch without this forming step; however, the I-V curve consistency was dramatically improved after allowing devices to operate at the 10 mA current compliance for a few cycles. For the RIE 200 sample, the first V_{SET} voltage did increase as the TE size decreased (Figure 4.4.4). A similar statement about the RIE 100 and 300 W samples cannot be made because of the "soft SETs."

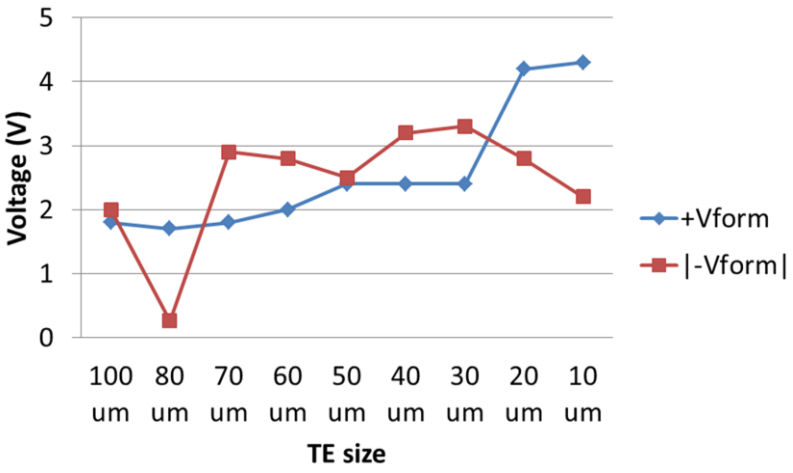


Figure 4.4.4 Initial V_{SET} data from RIE 200 W devices. $+V_{FORM}$ ($-V_{FORM}$) is the average initial $+V_{SET}$ ($-V_{SET}$) for two devices per TE size.

For this research, data were collected from two to four devices per TE size. Across all of the samples and device sizes, there were no observable trends between the switching styles, i.e. bipolar(+), bipolar(-), unipolar(+), unipolar(-), and the V_{SET} & V_{RESET} values. This did not preclude that different conduction and switching mechanisms may be at play for different switching styles, but any difference was neither readily apparent nor exacerbated at smaller TE sizes. Correlations were neither determined between the TE size and the V_{SET} & V_{RESET} values nor between the RIE power and V_{RESET} (Figure 4.4.5).

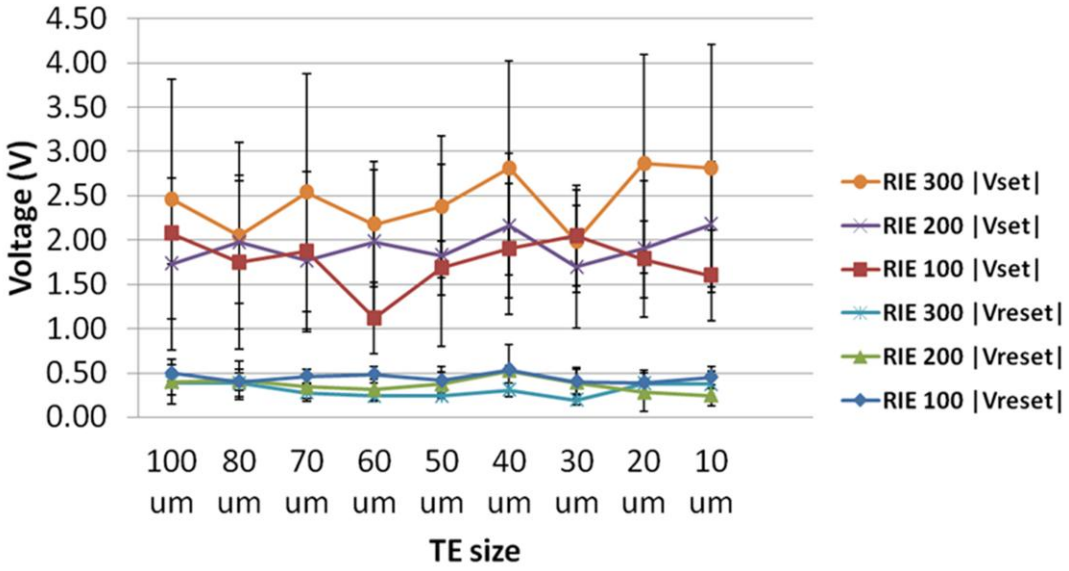


Figure 4.4.5 Plot of average V_{SET} & $|V_{RESET}|$ values across each RIE sample over the range of TE sizes. Graph indicates no significant trends for V_{SET} & V_{RESET} with respect to RIE power or TE size.

The initial HRS resistance of devices increased with decreasing TE size across all samples; however, the LRS resistance after the first V_{SET} did not trend with the TE size (Figure 4.4.6 a)). These relationships were also observed during normal device operation (Figure 4.4.6 b)). Sustained device switching continued, provided that the LRS resistance

was less than 100 Ω. If this condition was not met, the current compliance was increased until the LRS condition was met. This significance of this observation will be addressed later.

POX-43 (RIE 200 W) devices possessed greater HRS resistances than POX-44 (RIE 300 W) devices (Figure 4.4.6), yet the V_{SET} values of POX-44 devices tended to be greater than POX-43 devices (Figure 4.4.5). This clearly indicated that the V_{SET} value was not respective of the HRS value. Thus, the SET mechanism was likely not strongly dependent upon the current but the voltage itself.

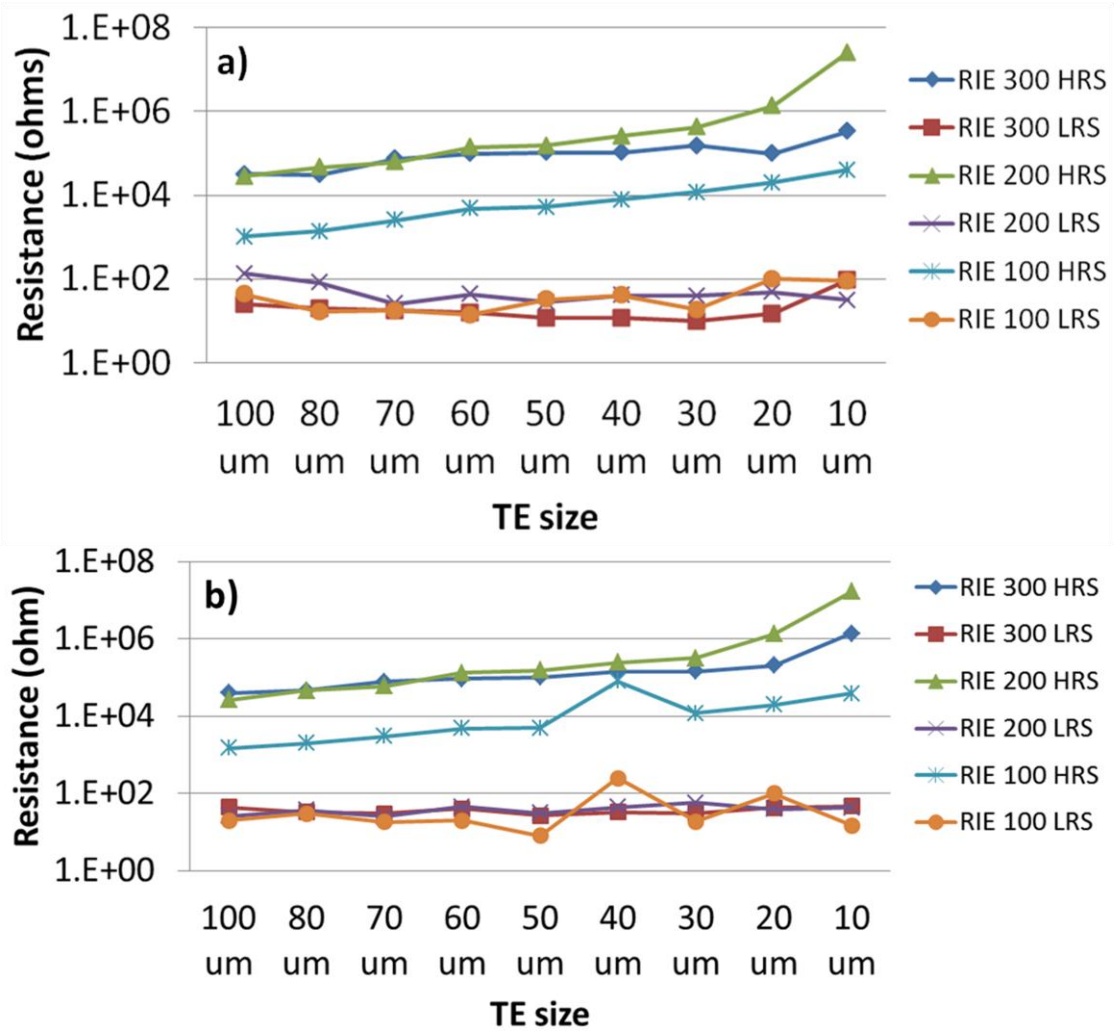


Figure 4.4.6 a) Plot of average initial HRS & LRS resistance values of samples with respect to TE size. b) Plot of average HRS & LRS resistance values of samples with respect to TE size during normal operation.

Additionally, the routine HRS per TE size was often less resistive or more resistive, ± (5-300)%, than the initial HRS. Under a filament creation/rupture device switching model, the initial resistance would be the maximum HRS resistance observed during the operation of the memristive device, since preexisting conduction paths were necessitated by the V_{FORM} step. It would then follow that the routine HRS resistance always would become less resistive than the initial HRS resistance in consequence of a more ordered

internal structuring following V_{FORM}, potentially related to a partial filament. Since changes to the HRS were not uniform, this suggested a more significant change in material structure during a SET/RESET beyond filament creation and rupture.

In the previous generations, a RESET operation tended to be as abrupt a resistance change as a SET operation. For the third generation devices, the RESET event was decidedly more gradual. In practice, this meant that a device could be partially RESET by sweeping out to a particular voltage (Figure 4.4.7), which is called a "staired RESET." Repeated sweeps to the same voltage did not significantly change the device resistance. Voltage sweeps of magnitude greater than the previous sweep enacted a resistance change. As is discussed in Section 4.5, ohmic conduction was observed along each leg of the voltage sweeps in Figure 4.4.7.

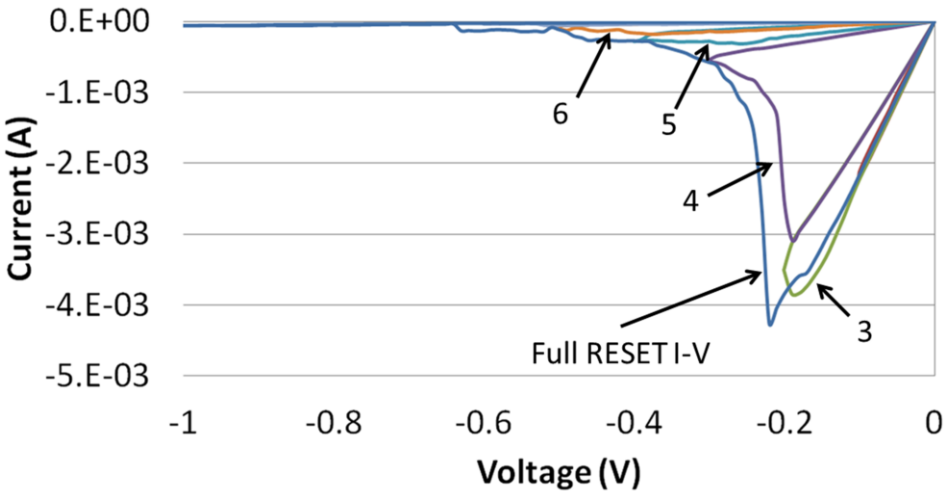


Figure 4.4.7 Staired RESET of RIE 300 W 60 µm square device. The full RESET I-V curve of a previous cycle is overlain on six staired RESET sweeps (only four such sweeps are labeled). The progression of these I-V curves clearly indicated a voltage based RESET mechanism as opposed to a flux or current based RESET mechanism.

All this was direct experimental evidence that a switching event was not incurred due to the accumulation of a threshold flux requirement. Nor was the RESET event a Joule heating (current driven) effect, since there was a strong dependence upon the voltage value in the resistance increase. Though not addressed in this research, these observations suggest that when these devices are operated using voltage pulses instead of voltage sweep, the magnitude of the voltage pulse will be more significant than the duration of the pulse.

The effect of the current compliance upon device operation was also tested. It was thought that high current compliances would create more conductive pathways and reduce the LRS resistance. Consequently, the conductive path would be more stable, requiring an increase in I_{RESET}. This more stable LRS may also affect the HRS resistance, which may have a role in determining V_{SET}.

One device from each of two different TE sizes was tested, but the data collected were consistent with general observations made throughout the device characterization experiments. Current compliance values of 0.5, 1, 5, and 10 mA were tested over five cycles each of bipolar(+) switching. It was expected that the higher current compliance values would cause more significant changes to the internal structure of the device. Thus the current compliances were tested from least to greatest.

The results of this test are listed in Table 4.4.2. For the 100 μm device, no drastic parameter changes were noted in either V_{SET}, V_{RESET}, I_{RESET}, HRS resistance, or LRS

resistance. The 50 µm device did see an increase in I_{RESET}, but did not have a corresponding decrease in LRS resistance.

Table 4.4.2 Effects of Icc upon bipolar(+) switching parameters

TE (µm)	V_{SET} (V)		V_{RESET} (V)		I_{cc} (mA)	I_{RESET} (mA)		HRS (kΩ)	LRS (Ω)
	min	max	min	max		min	max		
100	1.50	2.20	-0.22	-0.30	0.50	-8.00	-17.00	87	21
"	1.60	2.40	-0.25	-0.31	1.00	-10.50	-17.00	88	24
"	1.40	3.00	-0.46	-0.55	5.00	-10.00	-16.00	88	35
"	1.10	2.10	-0.41	-0.45	10.00	-12.00	-12.00	86	31
50	1.70	2.10	-0.22	-0.36	0.50	-3.50	-6.00	197	35
"	2.00	2.80	-0.24	-0.29	1.00	-3.00	-8.00	203	31
"	2.10	2.70	-0.29	-0.31	5.00	-6.50	-7.00	205	39
"	1.60	2.80	-0.29	-0.37	10.00	-9.50	-14.00	206	20

In practice, increasing the current compliance resulted in more consistent I-V switching curves. However, the specified current compliance value was software enforced. Since there was a delay between measuring a current above the specified limit and the control circuitry enforcing said compliance, it was very possible that the current overshoot was similar for any current compliance value. That is, the exact value may be less consequential than the mere fact that there was a limit to prevent a permanent electrical short.

Device endurance was tested with two POX-44 60 µm devices using bipolar(-) I-V sweeps. Pulse mode measurements would have been preferable given the digital logic domain of CMOS, but a pulse card was unavailable at the time. Endurance values of 171 and 238 cycles were obtained. In the first case, the LRS resistance failed to fall below

100 Ω, which was observed to be a minimum LRS resistance value to sustain device switching. In the second instance, V_{SET} travelled beyond the applied (-3) V applied bias.

Lastly, for all device operation hitherto discussed, the Cu film was grounded and the Al TE was biased. RIE 300 W 100 µm devices were cycled with the Cu BE biased and the Al TE electrically grounded. When operated in this manner, V_{SET} & V_{RESET} remained within their respective ranges reported for RIE 300 W 100 µm devices (Figure 4.4.3). This observation is addressed further in Section 4.5.

4.5 Conduction and Switching Mechanism

a) Theory

Due to the nature of plasma oxidation and the non-stoichiometric natures of the Cu_xO films created, particularly the second and third generation films, a significant number of positively charged oxygen vacancy point defects are expected, resulting in a *p*-type semiconducting material. Consequently, the injection and transport of the hole carriers of the Cu_xO will dictate the observed I-V behaviors of the metal-insulator-metal memristive devices [74, 75].

Upon the application of a voltage bias, while the number of thermally generated free carriers exceeds that of the injected charge carriers, ohmic conduction across the device will be observed. Once the injected charges exceed the thermally generated charges, the structures defects, traps sites, in the Cu_xO film become more significant.

SCLC describes the situation where unfilled traps inhibit electron conduction. Once all the trap sites are filled, electron flow is no longer trap-mediated, corresponding to a large increase in current [76]. For thick Cu_xO layers, SCLC was clearly demonstrated [74, 75].

For thin films, resistive switching was observed at voltages under 5 V. While this is a natural consequence of SCLC [46], Schottky emission [44] and the Poole-Frenkel (PF) effect [7] have also been observed for the HRS of memristive devices. Conduction sensitivity to electrode material for the HRS suggested an interfacial mechanism responsible for the various observations [77].

There are several methods for identifying the dominant conduction mechanism in the resistance states of a memristive device. For ohmic conduction, which follows $V = IR$, the slope, m, of the curve on a double logarithmic I-V plot is $m = 1$. SCLC is generally indicated by an increasing slope value as V increases, progressing from ohmic conduction to Child's Law, $I \alpha V^2$, ($m = 2$) and then to higher powers.

Schottky emission describes the increase of thermionic emission between a metal and a semiconductor by means of an electric field, which decreases the work function of the metal. Schottky emission may be described as [78]

$$\ln(J_S) = \frac{1}{2kT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}}\sqrt{E} + \left[\ln(A^*T^2) - \frac{q\phi_s}{kT}\right], \tag{4.5.1}$$

where J_s is the current density, q is the electron charge, ε_0 is the permittivity of free space, ε_r is the dielectric constant of the material, k is Boltzmann's constant, T is the Kelvin

temperature, E is the electric field, A^* is the Richardson constant, and ϕ_s is the barrier height. Based on Equation (4.5.1), Schottky emission is indicated as the dominant conduction mechanism when a plot of ln(I) vs. $V^{1/2}$ results in a linear slope.

The PF effect describes the emission of electrons from trap states in a material as a result of the reduced thermal energy requirements in the presence of a high electric field [78],

$$\ln\left(\frac{J_{PF}}{E}\right) = \frac{1}{kT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}}\sqrt{E} + \left[\ln(C) - \frac{q\phi_s}{kT}\right], \tag{4.5.2}$$

where C is a proportionality constant. Similar to above, plotting ln(I/V) vs. $V^{1/2}$ will result in a linear relationship if the device conduction is principally from the PF effect.

Lastly, in similar works, it has been hypothesized that Cu ions or oxygen vacancies form a conductive filament, resulting in a SET event, an LRS. Then upon a later sweep, the increased current would rupture the filament due to Joule heating [7].

b) Second Generation Cu_xO Devices

To elucidate the dominant conduction mechanism, switching and non-switching device I-V curves were plotted according to the tests above. For a representative virgin device, during the first SET, HRS conduction progressed from ohmic to PF emission before becoming ohmic during the LRS (4.5.1 a) & b)). The observed PF emission suggested a non-negligible number of trap states were influencing the conduction. Switching was not the result of merely filling the trap states as described by SCLC. During the RESET operation, the LRS followed ohmic conduction; but now the HRS also followed ohmic

conduction for the duration of the voltage sweep (Figure 4.5.1 c)) During routine operation, across all three samples, ohmic conduction was identified as the dominant conduction mechanism for both the LRS and HRS over both SET (Figure 4.5.2 a)) and RESET (Figure 4.5.2 b)) operations.

Ohmic conduction during the LRS was often attributed to filament formation of a conductive species [7, 49]; however, since an ohmic contact was observed in the HRS as well, the filament creation/rupture explanation was insufficient to account for the switching mechanism.

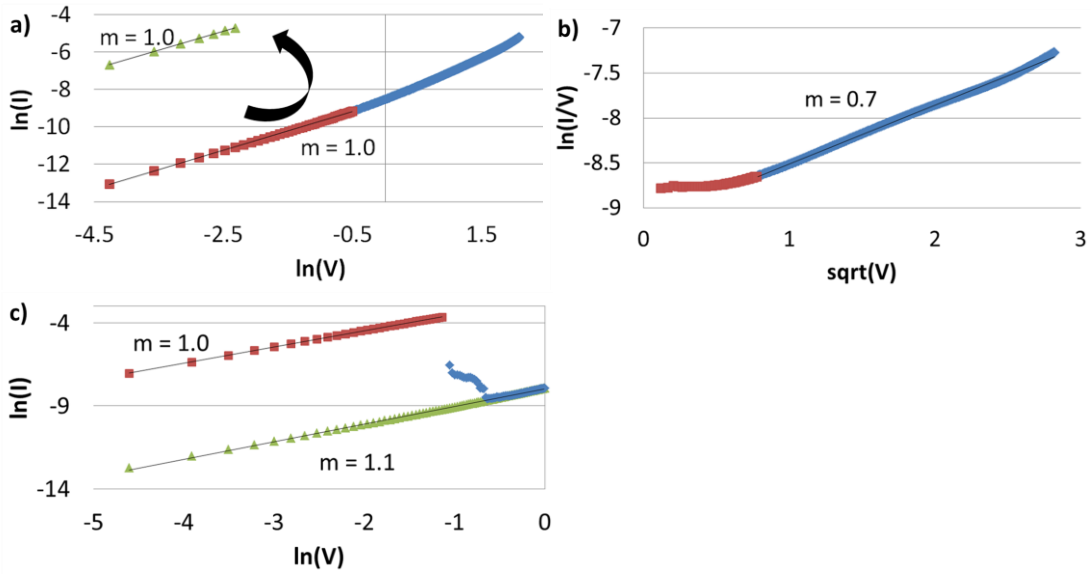


Figure 4.5.1 a) A double logarithmic I-V plot of the first SET, bipolar(-), of a RIE 300 W device clearly indicated ohmic conduction clearly indicated for the LRS and first part of the HRS leg of the curve b) PF effect conduction was indicated over the last stage of the HRS state during the SET operation. c) A double logarithmic I-V plot for the RESET operation clearly indicated as the dominant conduction method for both LRS and HRS

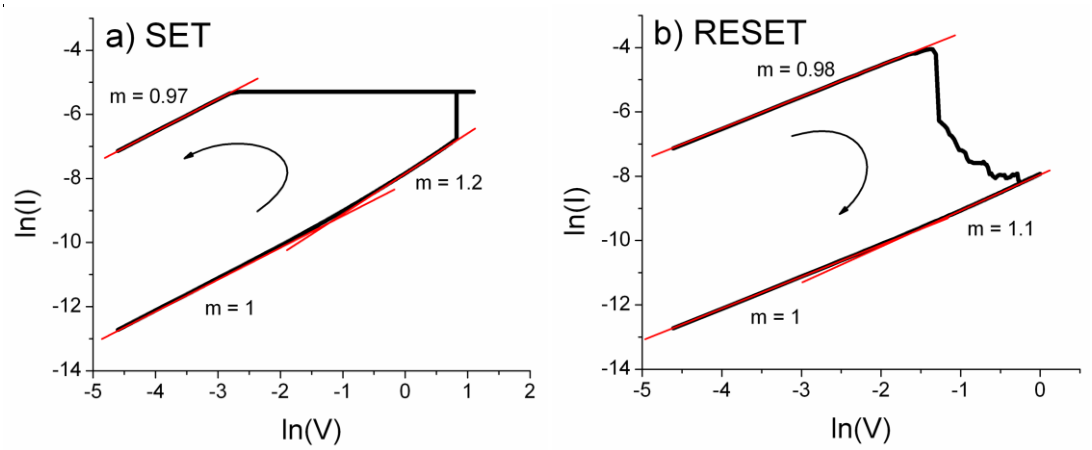


Figure 4.5.2 This figure shows the double logarithmic I-V plot of a RIE 300 W bipolar(+) device a) SET operation and b) RESET operation. Ohmic conduction was clearly indicated by the slopes of the curves as the dominant conduction method for both LRS and HRS in both a) and b).

An ohmic contact can form between a *p*-type semiconductor and a metal with a high work function, else a Schottky contact will result [79]. Given the work function of Cu_2O (4.84 eV), both Cu (4.35 eV) and Al (4.25 eV) should form Schottky contacts as fabricated. Since this is not observed, some phenomenon likely modified the interfacial regions. High dopant or defect state concentrations can also significantly alter contact properties [80]. Alternatively, a change to the chemical composition of the filament itself was a possible switching mechanism [81].

For non-switching devices of I-V behavior similar to Figure 4.5.1 b), the conduction mechanism also changed with the voltage. A double logarithmic plot of the I-V curve clearly indicated ohmic conduction as the principle conduction method at low voltages (Figure 4.5.3 a)). At higher voltages (>|1.5| V), however, the slope was decidedly non-linear. While the curve may be fit with multiple lines to suggest SCLC conduction

(Figure 4.5.3 a)), the transition points in SCLC were typically better defined, as shown in [47, 82]. There was a lack of strong linearity when the same data were graphed as ln(I) vs. $V^{1/2}$ (not shown), dismissing Schottky conduction. Finally, marked linearity is evident in the PF test plot, ln(I/V) vs. $V^{1/2}$ (Figure 4.5.3 b)), indicating this as the primary conduction method at high voltages for non-switching devices.

It is worth noting that while the majority of devices exhibited ohmic conduction in both the HRS and LRS, some devices still demonstrated PF effect conduction at high voltages (>|1.5| V). Since this was the conduction mechanism for virgin devices, it was thought that this indicated an inferior "formed" device compared to a device operating via ohmic conduction. It is not known what the key difference between non-switching and switching devices was at this time.

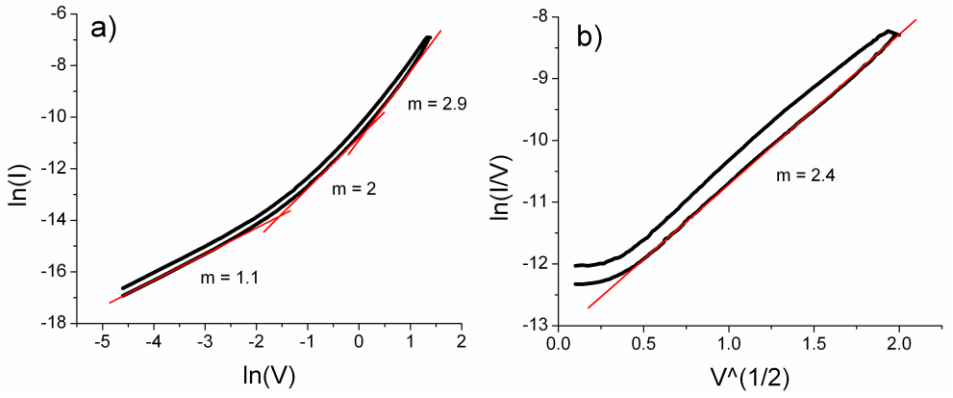


Figure 4.5.3 a) Double-logarithmic I-V plot clearly indicated ohmic conduction at low voltages. SCLC type fits may be imposed on the curve, but the transition points were not well defined. b) Poole-Frenkel emission clearly indicated in the figure.

To further analyze the LRS conduction mechanism, RIE 300 W devices that had been SET were measured at elevated temperatures. Decreasing LRS resistance during heating of a SET device generally indicates that the conduction path exhibited semiconducting behavior; whereas, increasing LRS resistance indicated a metallic conduction path. For these devices, the LRS resistance decreased 17% on average from 20° C to 145° C (not shown). These data suggested metallic filaments were unlikely present in the LRS.

For the RIE 100 W sample, the low power allowed for oxidation close to the surface, resulting in both a thin oxide and a 50:50 Cu:O ratio indicative of CuO. These results agree well with those reported by Lv, *et al.* [48], in which a CuO layer formed on the surface of copper oxidized in an oxygen plasma at similar conditions. At the RIE powers of 200 W and 300 W, the Cu:O ratio increased to 55:45 and 60:40, respectively. These results are consistent with Bellakhal, *et al.* [83], who showed that the composition of the resulting oxide shifted towards Cu_2O and Cu_3O_2 at RIE powers ranging from 200-300 W. While the oxide thickness did not increase monotonically with RIE power, in general, the lowest RIE power resulted in the thinnest oxide and the higher powers created thicker oxides. While more work is needed to statistically determine the exact thickness/power relationship, the increase in the oxide thickness with the RIE power can be explained by the increased energy of the oxygen ions increasing the oxidation depth.

The increase in the HRS resistance with the RIE power can be attributed to the composition of the oxide. Cu_2O is a known *p*-type semiconductor, as a result of oxygen vacancies; thus the oxide has a low resistivity. Conversely, CuO does not conduct as

well because of a reduction in vacancy concentration [84]. The thinnest oxide (RIE 100 W) was measured to be CuO; whereas, each successive oxide sample concentration further approached Cu_2O. This correlated with the significantly higher HRS resistance observed in the thinnest of the oxide films.

A unique and significant property of the devices fabricated in this research was the complete nonpolar switching behavior. Nonpolar behavior has been previously reported in Cu_xO memristive devices [7]; however, these investigators only showed evidence of bipolar(+) and unipolar(+) behavior, which by definition is not complete nonpolar behavior. While bipolar switching may be cursorily attributed to single species ion movement, the very similar $\pm V_{SET}$ values observed in this study suggest that 1) the SET mechanism is either polarity independent or 2) there are two separate polarity-dependent mechanisms present that are activated by similar voltage magnitudes. In the either case, the RESET mechanism has frequently been attributed to Joule heating due to high current flow, which is inherently polarity independent [7].

c) Third Generation Cu_xO Devices

The typical third generation Cu_xO device conduction mechanism did not differ from that of the second generation. Ohmic conduction was observed as the primary conduction method of both the HRS and the LRS; however, the staired and lateral switching of devices yielded additional insights.

The staired RESET provided a key window into the RESET mechanism of these particular devices (Figure 4.4.7). The voltage dependency indicated that neither magnetic flux from Chua's original equation nor current (Joule heating) were the primary RESET mechanism. A flux driven RESET would expect subsequent sweeps to an arbitrary voltage to increase the resistance (Section 2.1). Instead, the resistance value changed only when the applied bias exceeded the indicated V_{RESET} values. Furthermore, ohmic conduction was observed during each leg of the RESET (Figure 4.5.4). The continued Ohmic conduction did not indicate either band bending or trap emptying as a RESET mechanism. Rather, these data suggested evidence for a persistent filament through the device whether in the HRS or LRS, where the bistable resistive switching arises from changes in the composition of said filament by means of the electric field applied across it.

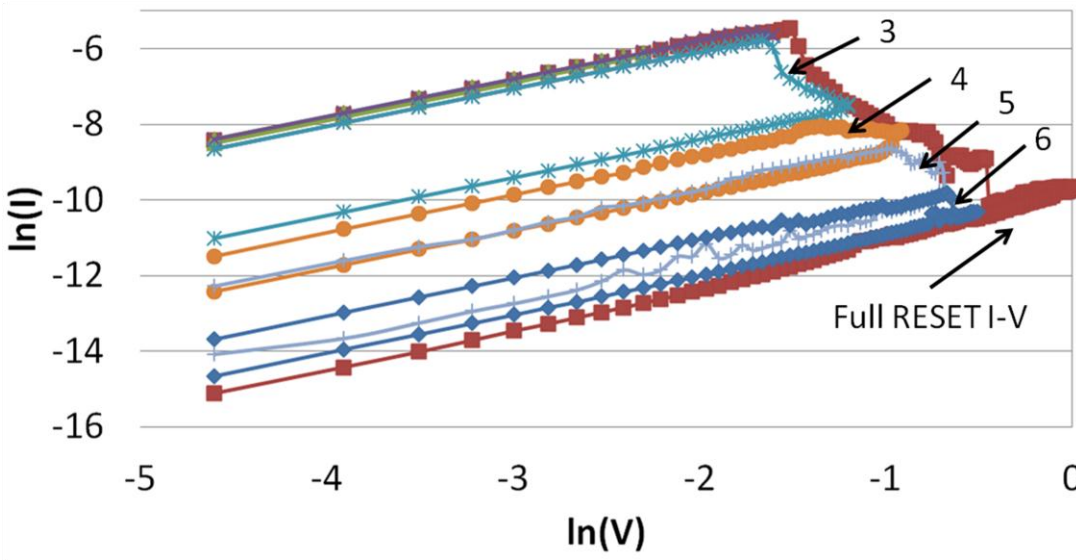


Figure 4.5.4 The double log I-V plot of HRS and LRS of Figure 4.4.7 clearly demonstrated that the slope of each leg of the four viable partial voltage sweeps was clearly ohmic, and the resistance does not change until the magnitude of the voltage sweep exceeded the previous sweep.

From Section 4.4 *b),* some POX-44 100 μm devices were cycled in which the Cu BE was biased and the Al TE was electrically grounded. Devices tested in this manner demonstrated complete nonpolar behavior. There was no obvious deviation of behavior from that of an Al TE biased, Cu BE grounded device.

In a representative virgin device, a conduction analysis of the first SET indicated ohmic conduction at low voltages (<1 V) (Figure 4.5.5 a)) before following a more Poole-Frenkel emission curve (Figure 4.5.5 b)). As seen in a routine I-V curve, ohmic conduction was observed as the primary conduction mechanism for both the HRS and LRS for both SET (Figure 4.5.6 a)) and RESET operations (Figure 4.5.6 b)). Since these results are the same for devices with biased Al TE, the switching mechanism was probably the same in both cases, independent of the biased metal layer.

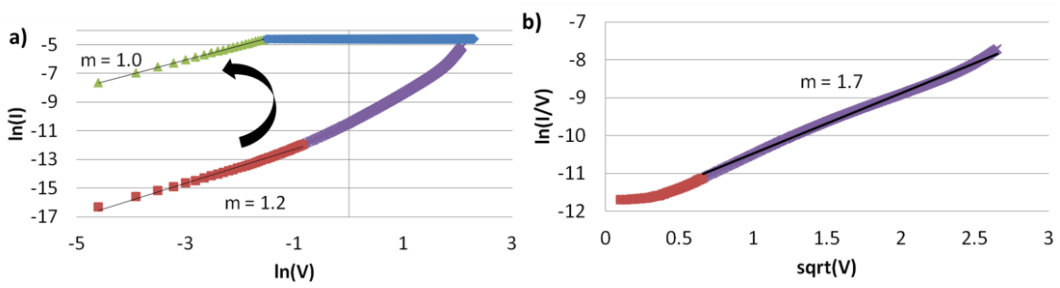


Figure 4.5.5 a) A double log I-V plot of a typical first SET of Cu biased, Al TE grounded device clearly indicated ohmic conduction for the first part of the HRS and the entirety of the LRS. b) Poole-Frenkel emission was indicated after the ohmic conduction for the HRS during the first SET.

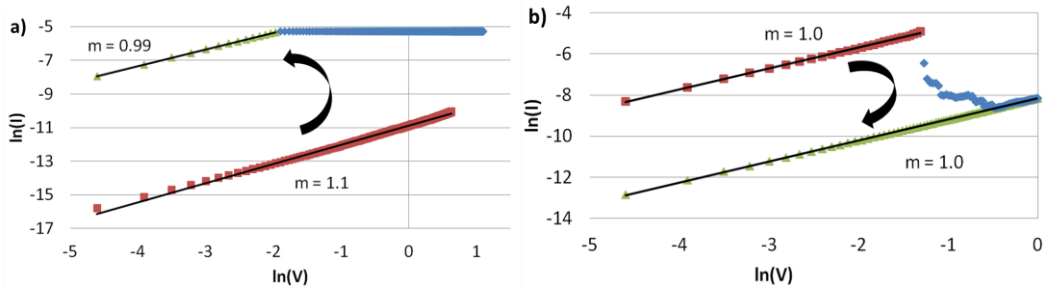


Figure 4.5.6 From a typical double logarithmic plot of a) SET and b) RESET operations for Cu biased, Al TE grounded devices, ohmic conduction was clearly indicated for HRS and LRS.

d) Lateral Switching Analysis

Thus far, it has been established that ohmic conduction was observed for both the HRS & LRS, which suggests a filament in both the HRS and LRS. Furthermore, a change to the filament itself is likely causing the switching and not the rupture & dissolution of the filament itself, as supported by the "staired" RESET. To procure unambiguous evidence for or against the creation/destruction of filaments during cycling, a lateral device switching routine was performed.

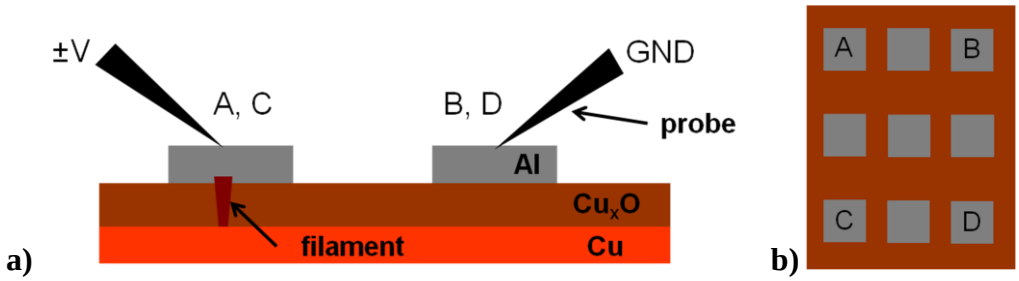


Figure 4.5.7 a) Figure depicts the side view of a memristive device under lateral switching. A voltage was applied to one TE while the other TE was grounded. b) An overhead view of device layout shows a 3x3 grid pattern indicated by the lettering. TE were separated 33 µm horizontally and 100 µm vertically.

Two sets of these lateral devices were considered per trial, viz. AB & CD. Since the physical separation of the TE might play a significant role in switching, these two lateral devices were spaced in three different configurations, 2x2, 3x3, and 4x4 (Figure 4.5.7 b)). TE pads were horizontally spaced 33 µm apart with 100 µm vertical separation. Each trial was conducted on a different grid to avoid the possibility of neighboring device switching interference. Probe tips were also confirmed indistinguishable by measuring all two probe combinations for lateral resistances measurements on a Cu test wafer.

After an initial vertical forming step (V_{FORM}), laterally switched device pairs AB & CD demonstrated the same complete nonpolar behavior observed in the vertically switched devices. As the separation distance between the TE increased, the minimum V_{FORM} increased (Figure 4.5.8 a)). V_{RESET} did not trend with the separation distance (Figure 4.5.8 b)). The minimum current compliance did increase from 0.5 mA to 2 mA as the grid size increased from 2x2 to 4x4. No other significant trends in the standard operating parameters were noted as a function of TE separation distance. Since complete nonpolar

behavior was observed even under lateral switching, it would be reasonable to expect similar switching mechanisms for both lateral and vertical operation.

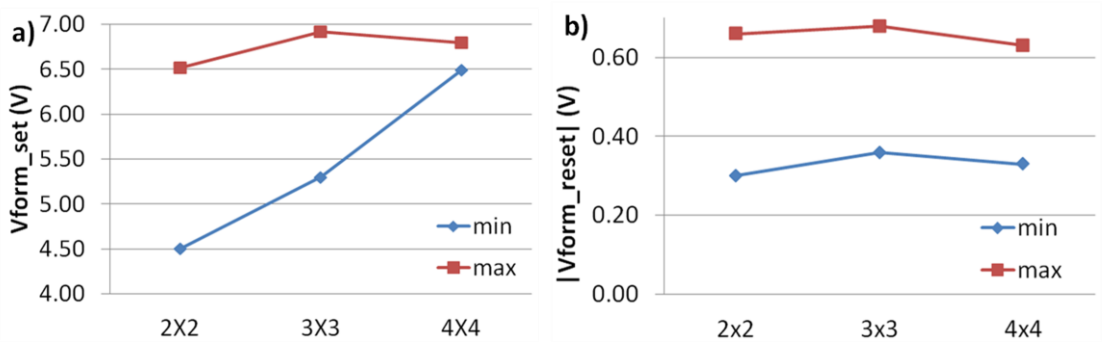


Figure 4.5.8 a) Plotting the V_{FORM} voltage as a function of grid size, an increase in the minimum V_{FORM} voltage as the TE separation distance increased was evident. b) However, the first V_{RESET} as a function of grid size indicated no dependencies on separation distance

Concerning the filament hypothesis directly, the resistance between four virgin devices was first measured laterally with a 100 mV read sweep in the following manner: AB, CD, AC, BD, AD, and CB, where the bias was applied to the first lettered TE and the second lettered TE was grounded (Figure 4.5.7 a)). As expected, all six resistance values were in the HRS (Figure 4.5.9 (1)).

Next, device AB & CD were SET with a 3 V sweep with a 0.5 mA current compliance (Figure 4.5.9 (2)). All six resistance values detailed previously were remeasured and indicated an LRS between each pair of TE indicating the existence of vertical conducting channels or "filaments" extending from the Al TE through the Cu_xO layer to the Cu BE

(Figure 4.5.9 (3)). If there were lateral filaments through the Cu_xO without touching the Cu layer, only the AB & CD measurements would have been in the LRS.

Next, device AB was RESET with a (-1) V sweep (Figure 4.18 (4)); and the six lateral devices were read again (Figure 4.5.9 (5)). It was evident from Figure 4.5.9 (5), that the LRS filament under the B TE persisted. Given two vertical filaments in a series circuit configuration, dual filament disruption was unlikely. If the filament change was voltage driven, then the voltage drop would be largest across the filament that first underwent a RESET process and returned to the HRS. By virtue of the large increase of resistance across the RESET filament, it is likely the voltage drop across the second lower resistance filament would be insufficient to cause filament disruption. If the RESET process was current driven, once one of the filaments returned to the HRS, the dramatic increases in resistance would prohibit current flow from disrupting the remaining filament.

It also bears noting that the HRS resistance increased by an order of magnitude from the initial HRS resistance. This further suggested a change in material structure during a SET/RESET beyond filament creation and rupture. It would be otherwise expected that the initial resistance would be the maximum HRS resistance observed during the operation of the memristive device, since there would not be preexisting conduction paths thereby necessitating the V_{FORM} step.

Lastly, device CD was RESET with a (-1) V sweep (Figure 4.5.9 (6)). All six lateral devices were remeasured. Persistent LRS filaments were unambiguously indicated under the B and D TE (Figure 4.5.9 (7)).

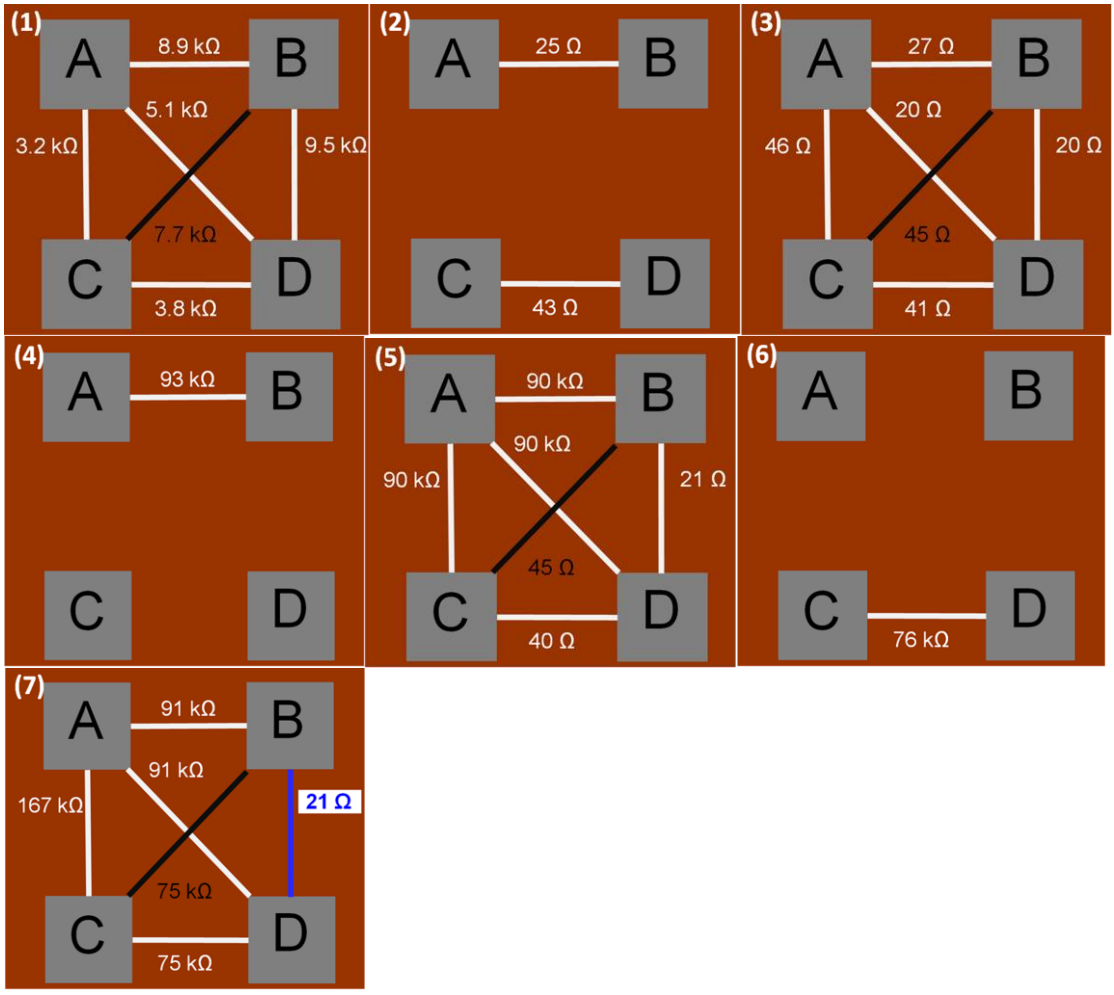


Figure 4.5.9 The persistent filament experiment procedure and experimental data was as follows: (1) measure initial resistance, (2) SET AB & CD, (3) read, (4) RESET AB, (5) read, (6) RESET CD, and (7) read. Step (7) clearly indicated persistent filament under the B & D TE.

Table 4.5.1 Persistent filament locations and grid size over multiple trials

	Filament locations			
Grid Size	A & C	A & D	C & B	B & D
2x2				X
3x3		X	X	X
4x4		X		X

Contrary to Kim, *et al.* [85], the locations of these persistent filaments in this work were not dependent upon the probe bias (Table 4.5.1). For example, persistent filaments were obtained under the B & D TE for AB & CD devices and for BA & DC devices.

Having shown evidence for the case in which only one filament returned to the HRS during a lateral RESET, it was desirable to determine if a pattern could be established that predicted the location of the persistent filament. To isolate contributing factors, the influence of adjacent device activity was first studied. At distances of at least 300 μm apart (TE edge to TE edge), cycling one device demonstrated no observable influence upon the resistance value of a neighboring device. Additionally, for a pair of devices cycled vertically and measured laterally, the laterally measured resistance value was merely the sum of the two vertically measured resistance values, i.e. resistors in series.

Two experimental procedures were devised for analyzing any influence LRS filament resistance had upon filament persistence. Two virgin devices 300 μm apart, A1 & A4, were both SET and read vertically. When the devices were read laterally, the total resistance was the sum of the A1 & A4 resistance values, consistent with previous observations. Next, the devices were RESET laterally, and A1 & A4 were read vertically (Table 4.5.2). The device with the least resistive filament returned to the HRS.

Furthermore, during subsequent cycles, the A1 filament remained the least resistive filament after each lateral SET and also continued to be the filament that returned to the HRS. However, it could not be determined if the A4 filament persisted because A1 was always the least resistive filament or because A1 was the first filament to return to the HRS, which established a precedent.

Table 4.5.2 Laterally cycled filament resistance values

	1) $R_{initial}$ (Ω)	2) R_{SET} (Ω)	3) R_{RESET} (Ω)
A1	101e3	34	104e3
A4	104e3	40	45

The significance of the least resistive filament reverting to the HRS during a RESET cannot be understated. This observation directly contradicts the popular explanation of Joule heating as the reason for the RESET behavior [7]. Joule heating comes from the power dissipated by the device, $P = I^2R$. In this circuit, Kirchhoff's current law necessitated the same current flow through both TE, thus

$$P_{A1} = I^2 R_{A1} < P_{A4} = I^2 R_{A4}. \tag{4.5.1}$$

In turn, the resistance of each filament is described by

$$R_{A1} = \frac{\rho_{A1}\ell}{A_{A1}} < R_{A4} = \frac{\rho_{A4}\ell}{A_{A4}}, \tag{4.5.2}$$

where ρ is the resistivity of the filament, ℓ is the length of the filament, and A is the cross-sectional area of the filament. Since the resistivity of the LRS filaments ought to be equivalent and it may be assumed that the filament lengths are the same (this assumption may be verified by cross sectioning the sample at a later date), it is reasonable to expect that the resistance of A1 was smaller than that of A4 because the former's filament

diameter was greater. Given this reasoning, it does not follow that Joule heating caused the thicker of the two filaments to change. The non-necessity of a Joule heating-based RESET was further supported by the observed staired RESET (Figure 4.4.7), where the resistance increased (current decreased) per subsequent voltage sweep.

The second experiment involved forming the first filaments via a lateral SET instead of a vertical SET. Laterally SET devices switched at similar voltages as vertically SET devices; however, in the former case, the voltage would be split between each device. Several scenarios were subsequently possible.

1) One filament formed completely first. After the first filament formed, most of the total voltage drop was applied to the other device, likely resulting in a thicker filament since a larger voltage was applied during the second SET. The latter has never been verified because the time resolution of the Agilent semiconductor analyzer is too slow to observe the formation of multiple filaments, though this observation is inconclusive.

2) Both filaments started forming contemporaneously and raced to the opposite electrode. In this case, since the starting electrodes may have been different, the composition of the filaments may have differed accordingly. As reported previously, the typical operating parameters of devices switched with a biased Cu electrode and electrically grounded Al TE were comparable to those of devices operated in the typical Al TE biased fashion (Section 4.4 *b)*). While this does not preclude different filament compositions, the effects of any differences are not readily apparent.

The most straightforward means to test each hypothesis would be to monitor the voltage across the Cu layer during device switching. For 1), the expected voltage would be half that of the applied and climb to the full applied bias as the first filament formed. For 2), the expected voltage would stay close to half the applied bias throughout the SET operation.

Alternatively, voltage sweeps of increasing magnitude could be applied laterally to a pair of devices, where the resistance of each individual device is read vertically after each sweep. In this manner, any changes in the vertical resistance may be seen as the sweep voltage approaches V_{SET}. Neither experiment has been performed at this time.

For the final filament experiment, several pairs of devices of varying separation distances (100 – 500 μm) were used. First, the device pairs were SET laterally, then each device was read vertically, and finally the pairs were read laterally. For devices SET laterally, the laterally read resistance was not equal to the sum of the vertical device resistance, unlike when the devices were first SET vertically. Instead, the lateral resistance values were either greater or less than the sum of each device individually. This observation is addressed later, but it may suffice for now, that likely a capacitive effect due to the floating Cu layer may account for these discrepancies.

Second, each pair of devices was laterally RESET. In all samples, the least resistive filament after the first SET returned to the HRS. Third, each pair of devices was

subsequently cycled laterally several times. Across all samples, the same filament that became highly resistive at the first RESET did so for all subsequent cycles, even if it was not the least resistive filament after any given SET. Thus, a persistence precedent was clearly established in this switching architecture.

The novelty of these results led to the application for a patent of the aforedescribed architecture for the purposes of truly random hardware one bit generation. For this invention, the location of the persistent filament between a pair of devices serves as the generated bit value. These devices are ideally suited for such applications as hardware identification and physically unclonable functions because the generated values are completely independent of each other, nonvolatile, and manufacturably irreproducible.

Currently, truly random number generators (TRNG), where each value is independent of previously generated values, are based on hardware component manufacturing variations. TRNG produce cryptographically optimal series; however, though the hardware is unique, previously generated series cannot be generated at will. Alternatively, pseudo random number generators (PRNG) utilize a seed value to generate numbers in a completely deterministic manner. Thus a series may be reproduced at will by anyone with the proper seed value [86]. These memristive devices provide the hardware unique values which are recallable on demand.

Since complete nonpolar switching was achievable with laterally cycled devices using operating parameters indistinguishable from vertical device operation, similar means of current conduction were expected to be employed. This hypothesis was incorrect.

The first SET of a RIE 300 4x4 virgin lateral device (Figure 4.5.10 a)) followed ohmic conduction (Figure 4.5.10 b)) before transitioning to Schottky conduction at higher voltages (>|0.5| V) (Figure 4.5.10 c)). LRS conduction was unambiguously ohmic in nature (Figure 4.5.10 b)). These conduction mechanisms, viz. ohmic then Schottky for the HRS & ohmic for the LRS, continued during routine nonpolar operation of devices in this manner. In some instances, ohmic only conduction was observed during the HRS of a RESET voltage sweep; in others, ohmic and Schottky emission were observed. There were no significant behavioral variations as a function of separation distance.

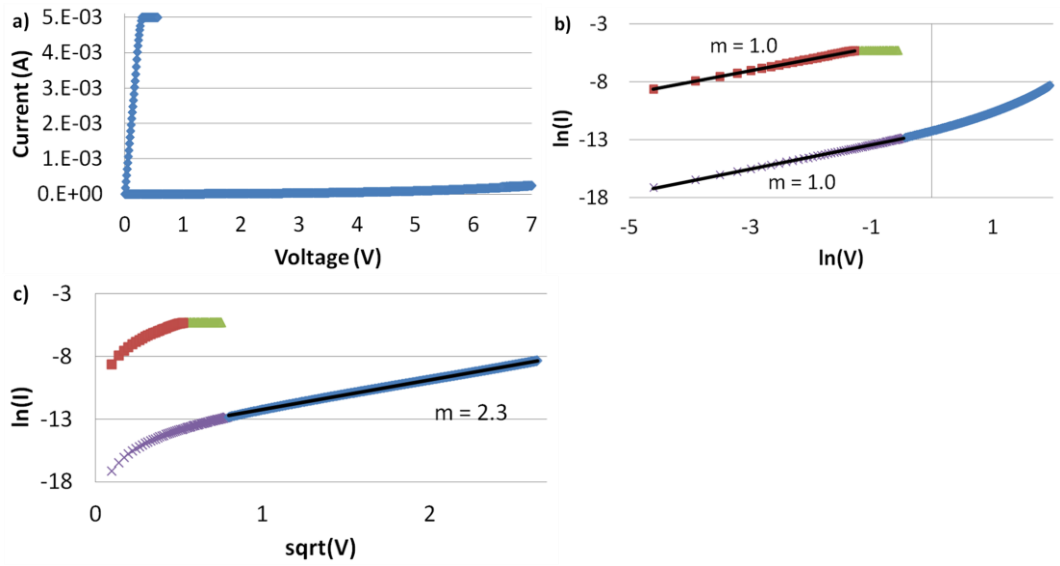


Figure 4.5.10 Analysis of the I-V plot of a) the first SET of lateral devices indicated b) ohmic conduction for the HRS at low voltages & LRS and c) Schottky emission following the HRS ohmic conduction.

It was previously mentioned that two vertically SET devices measured laterally behaved merely as resistors in series. However, devices operated only in a lateral fashion behaved dissimilar to resistors in series. The laterally measured resistance was either higher or lower than the sum of each device read vertically. This Schottky emission indicated in the conduction analysis accounted for this difference in the measured resistance, but it was still unclear why ohmic conduction changed to Schottky emission in this device configuration.

It was first considered that devices were characterized by biasing the Al TE and electrically grounding the Cu BE. During lateral device switching, one Al TE is grounded, where the Cu is left floating. To see if this electrical arrangement resulted in Schottky emission, devices were cycled while biasing the Cu BE and grounding the Al TE. The conduction analysis did not indicate Schottky emission but rather ohmic conduction.

An alternative hypothesis was that the floating Cu layer exhibits capacitive effects with the various material layers about it. Since the Cu layer is floating only in the lateral switching configuration, this would be consistent with the unobserved Schottky effect during vertical device cycling.

e) Switching Mechanism

From the presented data, it is put forth that the bistable resistive switching of Al/Cu_xO/Cu memristive devices arises from the composition modulation of a Cu_xO filament. At the first, ohmic conduction was observed to be the primary conduction mechanism for both LRS and HRS. A Schottky barrier was expected of this material stack but was unobserved, indicating an altered material arrangement at the interfaces.

It will be recalled that LRS ohmic conduction has been used to support the hypothesis of a conductive filament between the two metal electrodes during the LRS because ohmic conduction was then not observed during the HRS. This was explained as the result of the conductive filament rupturing due to Joule heating. Since ohmic conduction was present for both the LRS and HRS and not to the same extent during the first SET of a virgin device, it is expected that 1) a filament is created during the first SET and 2) the filament persists in some form after the RESET operation, creating a new HRS resistance value which may greater or smaller than the initial HRS resistance.

The existence of filaments was unambiguously confirmed in the lateral switching experiments, indicating a vertical filament beneath the TEs. Further, the lateral RESET event further demonstrated that no filament was rupturing due to Joule heating, since the least resistive filament changed. Further, RESETs have been repeatedly observed to occur over a narrow voltage range and not between a similarly narrow current range, strongly suggesting a voltage driven RESET. The “staired” RESETs strongly indicate a voltage driven effect because resistance increases incrementally with respect to the maximally attained voltage value and not the achieved current level.

The LRS resistance measurements at elevated temperatures indicated a semiconducting filament, ruling out a Cu ion filament. However, it has already been shown that the resistance difference between Cu, CuO, and Cu_2O is quite significant. Considering also the change in HRS resistance following the first SET/RESET cycle, a semiconducting filament of changing Cu:O ratios modulated by the applied voltage bias satisfies all the above noted properties and behaviors.

During the initial SET, V_{FORM}, ohmic conduction is initially observed due to thermally generated carriers. At elevated voltages, PF conduction allows more electrons to travel. The increased current and electric field has already been reported to cause ions and vacancies to become mobile [87]. In this manner, a filament of composition between Cu_2O and pure Cu is generated. (Obviously, a pure Cu filament is not completely achieved during a SET as indicated by the elevated temperature experiments in Section 4.5 *b).*) This ratio comes from the observed sub-100 Ω LRS resistance.

This filament generation relies on both Cu ion and oxygen vacancy displacement, both of which are positively charged. However, the difference between the HRS and LRS filament composition need not be drastic to produce large resistance changes. As seen in Figure 4.5.11 a), a SET I-V curve rapidly transitions between two conduction states, clearly indicates an internal structure to its oscillations. Another example of this is seen in Figure 4.5.11 b), which shows four different conduction states of the device during a failed SET operation.

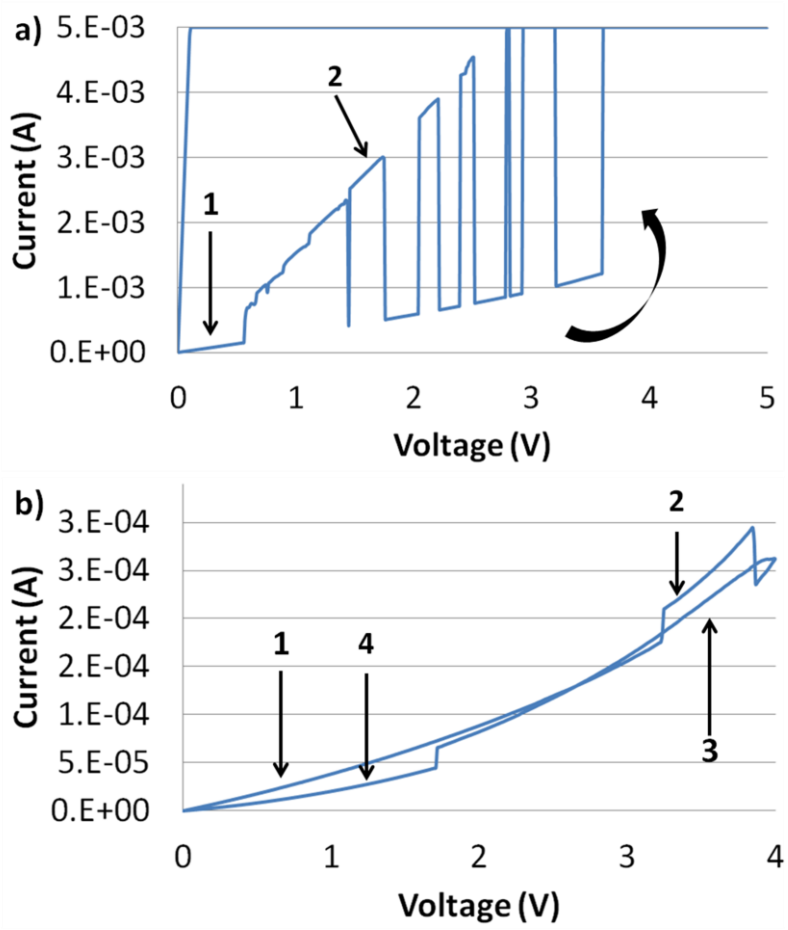


Figure 4.5.11 a) Repeated oscillation between two well defined conduction states during one voltage sweep clearly indicated internal structure to the device prior to the transition to the LRS. b) Similarly, four separate conduction curves were observed in one device which failed to SET. These data suggest a filament composition change during SET/RESET operations.

4.6 Summary

Al/Cu_xO/Cu memristive devices were fabricated and characterized for the purposes of eventual inclusion into standard CMOS technology. Plasma oxidation was employed to grow the Cu_xO films used. The RIE power was shown to directly affect the final oxide

thickness and oxygen concentration. The oxygen concentration was shown to correlate with the HRS resistance of these devices.

Second and third generation memristive devices demonstrated complete nonpolar switching behavior for both vertical and lateral device measurements and were generally operable with voltages <|3| V and currents under 20 mA. The HRS and LRS both followed ohmic conduction. Stepped switching was also demonstrated. Date suggested a voltage driven switching mechanism based on composition modulation of a Cu_xO filament. Lastly, a patent was submitted based on the results of this research concerning the lateral switching for use in hardware based truly random one bit generation.

V. Modeling & Simulation of Memristive Devices

5.1 Introduction

Typical devices models rely on lookup tables for the expected output, but memristive device models must take into account immediate as well as past conditions to output an accurate result. At the same time, the model ought not to be computationally intensive, else large scale simulations incorporating potentially $10^6 – 10^9$ memristive devices would be untenable.

When Hewlett-Packard (HP) first announced their memristive devices, two serial resistors were proposed as a model to replicate the hysteretic behavior of one memristor [3]. This boundary drift model (i.e. ratio between a large and small resistor in series) served as a rough equivalent to the hypothesized expanding and contracting of the vacancy laden region inside a titanium oxide based device. While this simplistic model is still used today in purely academic simulations, the model has proved unsuitable for replicating the behaviors of a majority of real memristive devices.

To improve the linear boundary drift model, a more physics based non-linear component was added to the boundary drift equation [72, 73]. The intent of the boundary drift models was to describe device behavior with respect to various explicit physical parameters. The complexity of the model may increase the range of reproducible device behaviors, but it may also prove to be too difficult to determine the appropriate parameter values for an arbitrary device. Thus an empirical model was developed to allow for rapid reproduction of experimental I-V curves for the purposes of incorporation with CMOS

circuit simulation software.

5.2 Boundary Drift Models

a) Linear Boundary Drift Model

The linear memristor device model reported by Hewlett-Packard (HP) [3, 41] stated that the effective transport mechanism in TiO_2 based memristive devices was through the drift of vacancies originating within an oxygen deficient TiO_{2-x} layer [3]. As described by Pickett *et al*. [88], oxygen vacancies drifted under an applied external electric field, thus the stoichiometric TiO_2 became doped with the ionized vacancies.

Treating the doped (oxygen vacancy rich regions) and undoped regions of the device as a pair of resistors in series, the memristance corresponding to a given boundary position or state, *w*, relative to the device length or thickness *D* (Figure 5.21) was described as follows [3]:

$$M(w) = R_{on}\left(\frac{w}{D}\right) + R_{off}\left(1 - \frac{w}{D}\right), \tag{5.2.1}$$

where R_{on} is the resistance of the doped region and R_{off} is the resistance of the undoped region.

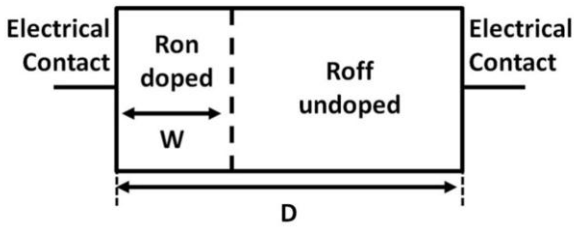


Figure 5.2.1 Figure depicts schematic representation of the memristor device as two resistors in series.

The drift velocity, v_D, at which the doped/undoped boundary interface moved was defined as [72]

$$\frac{\mathrm{d}w}{\mathrm{d}t} = v_D = \frac{\eta\, \mu_D\, R_{on}}{D}\, I(t), \tag{5.2.2}$$

where the oxygen vacancies had a characteristic drift mobility, μ_D, under any applied bias voltage. η indicated the polarity of the memristor, where η = 1 or -1 for a device whose doped region was expanding or shrinking respectively under a positive voltage bias. For example, the memristor device in Figure 1 has an η = 1 polarity, i.e. bipolar(+).

Integrating both sides of Equation 5.2.2 gave the state *w* as a function of time [72]

$$w(t) = w_0 + \frac{\eta\, \mu_D\, R_{on}}{D}\, q(t), \tag{5.2.3}$$

letting $q(0) = 0$. Substituting Equations 5.2.3 into 5.2.1, the device's memristance, *M*, may be solved for as a function of charge [72]

$$M(q) = R_0 - \frac{\eta\, \Delta R}{Q_0}\, q(t), \tag{5.2.4}$$

where, after grouping terms, the parameters R_0, Q_0, and ΔR were given by [72]

$$R_0 = R_{on}\left(\frac{w_0}{D}\right) + R_{off}\left(1 - \frac{w_0}{D}\right), \tag{5.2.5}$$

the initial resistance of the memristor;

$$Q_0 = \frac{D^2}{\mu_D\, R_{on}}, \tag{5.2.6}$$

the charge required to alter the state from w_0; and

$$\Delta R = R_{off} - R_{on}\,. \tag{5.2.7}$$

From Chua's seminal memristance equation [8]

$$d\varphi = M\, dq, \tag{5.2.8}$$

one may derive essentially Ohm's Law,

$$M\big(q(t)\big) = \frac{d\varphi/dt}{dq/dt} = \frac{V(t)}{I(t)}. \tag{5.2.9}$$

Using Equation 5.2.4, Equation 5.2.9 may be rewritten as [72]

$$V(t) = \left[R_o - \frac{\eta\, \Delta R}{Q_0} q(t)\right] \frac{dq}{dt}. \tag{5.2.10}$$

Then integrating Equation 5.2.10 with respect to time, one could solve for the magnetic flux

$$\varphi(t) = R_o q(t) - \frac{\eta\, \Delta R\, q^2(t)}{2Q_0}, \tag{5.2.11}$$

which, in turn, provided an equation for $q(t)$ via its quadratic solution [72]

$$q(t) = \frac{Q_0\, R_0}{\Delta R}\left(1 - \sqrt{1 - \frac{2\eta\, \Delta R\, \varphi(t)}{Q_0\, R_0^2}}\right), \tag{5.2.12}$$

again letting $q(0) = 0$. Substituting Equations 5.2.12 into 5.2.4, one obtained an equation for memristance explicitly as function of the flux [72]

$$M(q) = R_0 \sqrt{1 - \frac{2\eta\, \Delta R\, \varphi(t)}{Q_0\, R_0^2}}. \tag{5.2.13}$$

Finally, by inserting Equation 5.2.13 into Equation 5.2.9, one could solve for the current flowing through the memristor device [72]

$$I(t) = \frac{V(t)}{R_0 \sqrt{1 - \frac{2\eta\, \Delta R\, \varphi(t)}{Q_0\, R_0^2}}}. \tag{5.2.14}$$

The linear boundary drift model assumed that the oxygen vacancies were free to traverse the entire length of the memristor unhindered by the boundary conditions of the device. The utility of this model lay within the ease of usage and closed form solution.

b) Non-linear Boundary Drift Models

The linear boundary drift model reproduced the characteristic hysteretic behavior of memristors; however, the model suffered from oversimplifications of basic electrodynamics. First of all, even small voltages across the nanometer devices will produce a large electric field; thus the ion boundary position will move in a decidedly non-linear fashion. Additionally, w could never achieve a zero length in practice. Such an event would indicate that there were physically no oxygen vacancies present in the device, the identified charge carriers. On the other hand, the entire length of the device could potentially become doped with the oxygen vacancies. Modeling the state change as a mass on a spring, the boundary drift velocity, v_D, should be greatest at the center of the device and reduced to essentially zero as w approached either edge ($w = 0$ and $w = D$). These boundary value restrictions were implemented by multiplying a windowing function to Equation 5.2.2 as shown below [72, 73]

$$v_D = \frac{\mathrm{d}w}{\mathrm{d}t} = \frac{\eta\, \mu_D\, R_{on}}{D}\, I(t)\, F(x), \tag{5.2.15}$$

where $x = w/D$ is the normalized form of the state variable. The function $F(x)$ should have its highest value at the center of the device ($x = 0.5$) and be zero at the boundaries, $x = 0$ and $x = 1$. Joglekar *et al.* [72] proposed the window function

$$F_p(x) = 1 - (2x - 1)^{2p}, \tag{5.2.16}$$

where p is a positive integer. Figure 5.2.2 displays a graphical representation of the window function described by Equation 5.2.16 for various p solutions ($p = 1$, 5, and 10). From the figure, it is evident that the maximum $F_p(x)$ value occured at the center of the device and that zero values were obtained at the two boundaries. Also, by varying the p

parameter, the rate of change of the function could be tuned. Lower p values corresponded to lower rates of change and vice versa. Inserting Equation 5.2.16 into Equation 5.2.15, the modified state change equation was obtained

$$\frac{\mathrm{d}w}{\mathrm{d}t} = \frac{\eta\, \mu_D\, R_{on}}{D} I(t)[1 - (2x - 1)^{2p}]\,. \qquad (5.2.17)$$

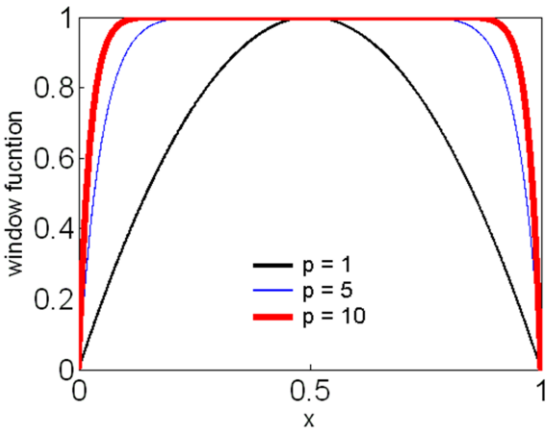


Figure 5.2.2 Figure depicts plot of non-linear window function proposed by Joglekar *et al.* for p = 1, 5, and 10.

It may be observed that Equation 5.2.17 reduces to the linear boundary drift model described by Equation 5.2.2 as p increases [72]. Equation 5.2.17 also utilized the η parameter since the Figure 5.2.1 memristive device is asymmetric. During modeling and simulation, each device's physical orientation would become significant given the switching described mechanism.

The non-linear state change model described by Equation 5.2.17 was more physically accurate when compared to the linear model; however, the window function made solving for w as function of time nontrivial for an arbitrary p. Therefore, a time-step

numerical solutions approach was employed for simulations. The following formulae were independently derived from the algebraic manipulation of Equations 5.2.1, 5.2.9, and 5.2.17 as shown below

$$M(w(t_i)) = R_{on}\left(\frac{w(t_i)}{D}\right) + R_{off}\left(1 - \frac{w(t_i)}{D}\right), \quad (5.2.18)$$

$$I(t_{i+1}) = \frac{V(t_{i+1})}{M(w(t_i))}, \quad (5.2.19)$$

$$v_D(t_{i+1}) = \frac{\eta\, \mu_D R_{on}}{D} I(t_{i+1})\, F_p\left(\frac{w(t_i)}{D}\right), \quad (5.2.20)$$

$$w(t_{i+1}) = v_D(t_{i+1})[t_{i+1} - t_i] + w(t_i), \quad (5.2.21)$$

$$q(t_{i+1}) = \Phi(t_{i+1}) / M(w(t_i), \quad (5.2.22)$$

where t_i in Equation 5.2.18 corresponds to the initial time step and t_{i+1} in Equations 5.2.19 - 5.2.22 the next integral time step.

The order of these time-step equations brought to light another challenge in the implementation of Equation 5.2.16, specifically when the doped region covered the entire device length (x = 1). It then followed that $F_p(x = 1) = 0$ for all p, Equation 5.2.16. Thus, w in Equation 5.2.21 would not change since $v_D = 0$, Equation 5.2.20. Therefore, x = 1 once again for the next time-step during simulation. This loop then persisted till the end of the simulation without respect to the change in the direction of the current, generating invalid results.

A new window function was proposed by Biolek *et al.* [73]

$$F_p(x) = 1 - \left[x - \mathrm{u}(-I)\right]^{2p}, \quad (5.2.23)$$

where

$$u(I) = \begin{cases} 1, & \text{if } I \geq 0 \\ 0, & \text{if } I < 0 \end{cases}. \tag{5.2.24}$$

This window function is displayed in Figure 5.2.3 for various p integer values (p = 1, 5, and 10). The state change was no longer modeled as a mass on a spring; rather, the function was asymmetric in the way it restricted the rate of change in v_D. For example, when x started at 0, the function equaled 1. Then, as x increased, approaching D, the function approached 0. Once the current reversed direction, the function immediately switched to 1. Then, as x decreased back to 0, the function also decreased to 0. When the current reversed, the cycle began anew. The key advantage of Biolek's window function was that it eliminated convergence issues at the device boundaries. In order to compute v_D, Equation 5.2.23 was substituted into Equation 5.2.20 without altering the other four equations.

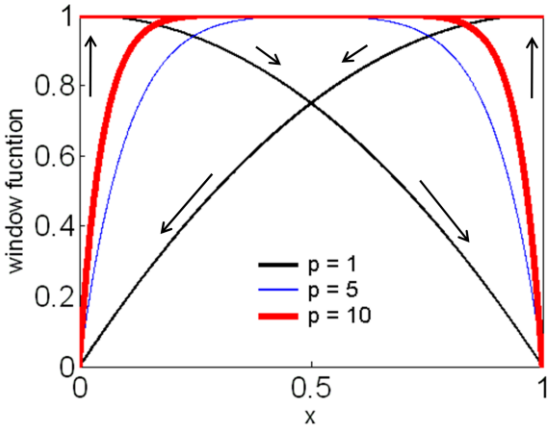


Figure 5.2.3 Figure depicts plot of non-linear window function proposed by Biolek *et al.* for p = 1, 5, and 10.

c) Boundary Drift Model Comparison

During model analysis and simulation, all memristor models were simulated in MATLAB; and all bias voltage sources were sinusoidal

$$V(t) = v_0 \sin(\omega_0 t + \theta), \tag{5.2.25}$$

where v_0 is the voltage amplitude and θ is an arbitrary phase shift. Typical simulation input parameter values were v_0 = 1 – 5 V and ω_0 = 10 – 10^6 rad/s. The flux through the device was simply the time integral of the voltage across it from Equation 5.2.25

$$\Phi(t) = \left(\frac{v_0}{\omega_0}\right) [\cos\theta - \cos(\omega_0 t + \theta)]. \tag{5.2.26}$$

i) Linear Boundary Drift Model

The physical memristor device as described by Strukov, *et al.* [3] was characterized by the parameters μ_D, w_0, D, R_{off}, and R_{on}. Adjustments to the dopant mobility parameter directly correlated to changes in the boundary drift velocity as described in Equation 5.2.2. A slower (faster) velocity corresponded to smaller (larger) changes in w per cycle, which in turn decreased (increased) the resistance value spectrum available to the memristive device. Adjusting w_0 also directly altered the effective range of resistance values available to the memristor. In general, a higher w_0 produced wider loops in the *I-V* plots. However, neither μ_D nor w_0 could be set to completely arbitrary values; otherwise, imaginary numbers arose in the equations. Overall, the model operated over the widest range of parameter values when the initially doped region was less than half the device length. The maximum viable μ_D and w_0 values were modulated by the frequency of the voltage source, where frequencies on the orders of tens of hertz allowed for larger values in both parameters. Devices with high D values displayed less memristive effects than

short devices because, according to Equation 5.2.4, memristance falls off as an inverse square function.

The R_{off} and R_{on} resistance values could be arbitrarily set in accordance with their definitions. The ratio $r = R_{off}/R_{on}$ should at a minimum be greater than 10. Ratios of r = 100 – 2000 were typically commonly used. Increasing r generally reduced the *I-V* curve to a straight line. Additionally, for any given D, hysteresis effects were most prominent when $\Delta R >> R_0$ [72]. For the linear state change model, typical parameters were μ_D = (10^{-12} – 10^{-14} $m^2 \cdot V^{-1} \cdot s^{-1}$), D = (10 – 50 nm), x_0 = (0.1 – 0.6), R_{on} = (100 – 1000 Ω), and r = (100 - 2000).

Figure 5.2.4 shows typical simulation results. Figure 5.2.4 a) superimposes the input voltage in time (thin line) against the current in time (thick line). From the plot, it is apparent that while the current lagged the voltage, both curves had the same period. This indicated that the memristor did not store any charge itself but was a totally dissipative circuit element [8]. Figure 5.2.4 c) depicts the symmetric, smooth hysteresis loop of an ideal memristor. Figure 5.2.4 b) & d) show the variation in width w and memristance over time, respectively. From the figures, when w was greatest, memristance was minimum and vice-versa; both parameters mirror each other.

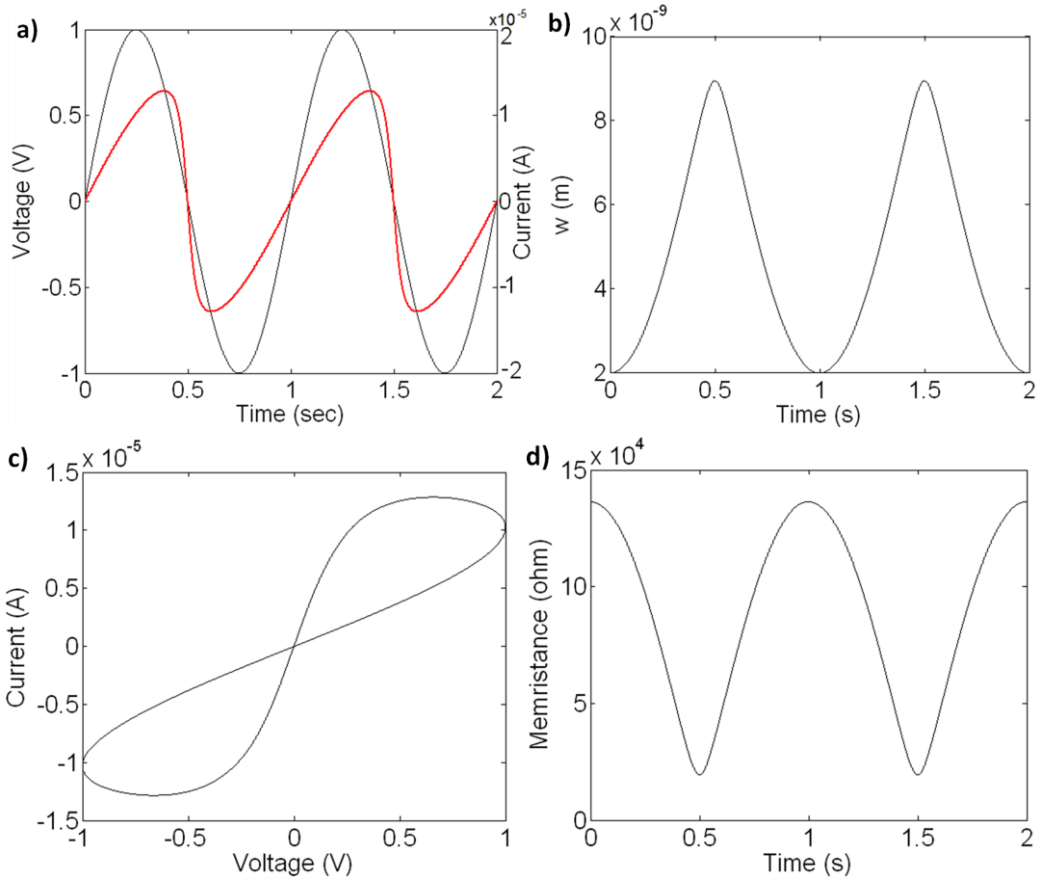


Figure 5.2.4 Figures are of a) $I(t)$ & $V(t)$, b) $w(t)$, c) V-I hysteresis behavior, and d) $M(t)$ memristor simulation results using the linear boundary drift model, with parameters $\mu_D = 10^{-14}$ $m^2V^{-1}s^{-1}$, $D = 10$ nm, $x_0 = 0.2$, $R_{on} = 1700\ \Omega$, $r = 100$, $v_0 = 1$ V, $\omega = 2\pi$ rad/s, and $V(t) = \sin(2\pi\, t)$ V.

ii) Non-linear Boundary Drift Models

For modeling and simulation of non-linear memristor models, the optimal time-step values, $\Delta t = t_{i+1} - t_i$, were determined to be between 10^{-2} – 10^{-4} sec. The model simulation results using Joglekar's window function are shown in Figure 5.2.5. The I-V plots exhibit a more pointed signature (Figure 5.2.5 a) & c)) compared to the linear model results (Figure 5.2.4 a) & c)). While both $I(t)$ plots had the same period as their respective voltage inputs, the former were sharper because of the usage of the window

function. It was also observed that for high p integer values ($p > 20$), the non-linear model behaved as its linear counterpart (not shown). Note, the memristance and w plots remained similar for both linear (Figure 5.2.4) and non-linear models (Figure 5.2.5).

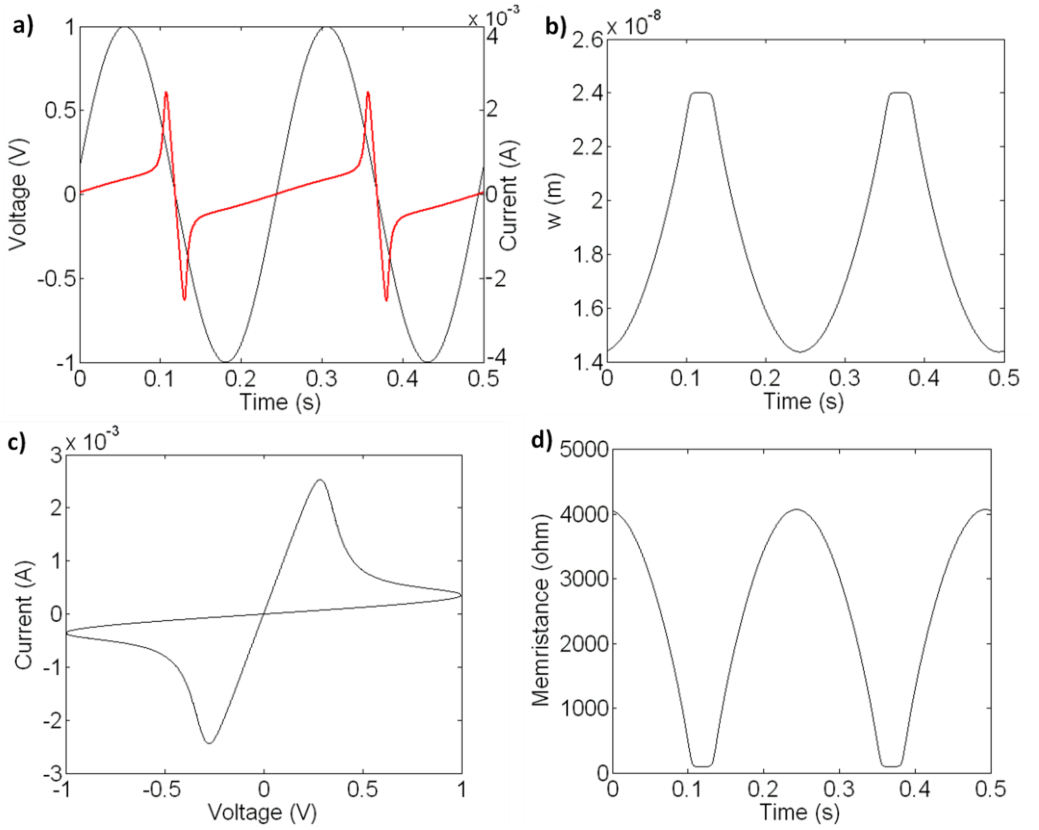


Figure 5.2.5 Figures are of a) $I(t)$ & $V(t)$, b) $w(t)$, c) V-I hysteresis behavior, d) and $M(t)$ memristor simulation results using non-linear dopant drift model and Joglekar's window function, with parameters μ_D = 6.4 x 10^{-14} $m^2V^{-1}s^{-1}$, D = 24 nm, w_0/D = 0.6, R_{on} = 100 Ω, r = 100, p = 7, v_0 = 1 V, $\omega = 8\pi$ rad/s, $V(t) = \sin(8\pi t + 0.16)$ V, $\Phi(t) = \left(\frac{1}{8\pi}\right)[\cos(0.16) - \cos(8\pi t + 0.16)]$ Wb, and $\Delta t = 10^{-4}$ sec.

Under certain sets of parameters, the memristor fluctuated for a few cycles before settling on a consistent pattern of behavior. However, setting an appropriate phase shift eliminated these initial fluctuations. A phase shift of 0.16 rad was employed during the

simulation in Figure 5.2.5. The window function also increased the model's robustness in terms of arbitrary parameter range selection. Lastly, in terms of parameter selection and adjustment, both linear and non-linear models were similarly affected.

In terms of simulation stability, certain non-linear model simulations could not be performed for an arbitrary length of time when employing Joglekar's window function. This failure was caused by the convergence issue described in Section 5.2 *b)*. To partially remedy this problem for additional simulation time, one could increase *D* (up to around 50 nm, maintaining physical dimensions). However, this was not a comprehensive solution.

Simulation results employing Biolek's window function (Figure 5.2.6) preserve the highly non-linear characteristic device behavior without the convergence problems. In addition, Biolek's model was unique because it allowed for general asymmetric I-V device behavior modeling, which was not realizable except under extreme circumstances with the two previous models. This was significant because typical physical memristor experimental data [3, 88] exhibited asymmetric I-V behavior.

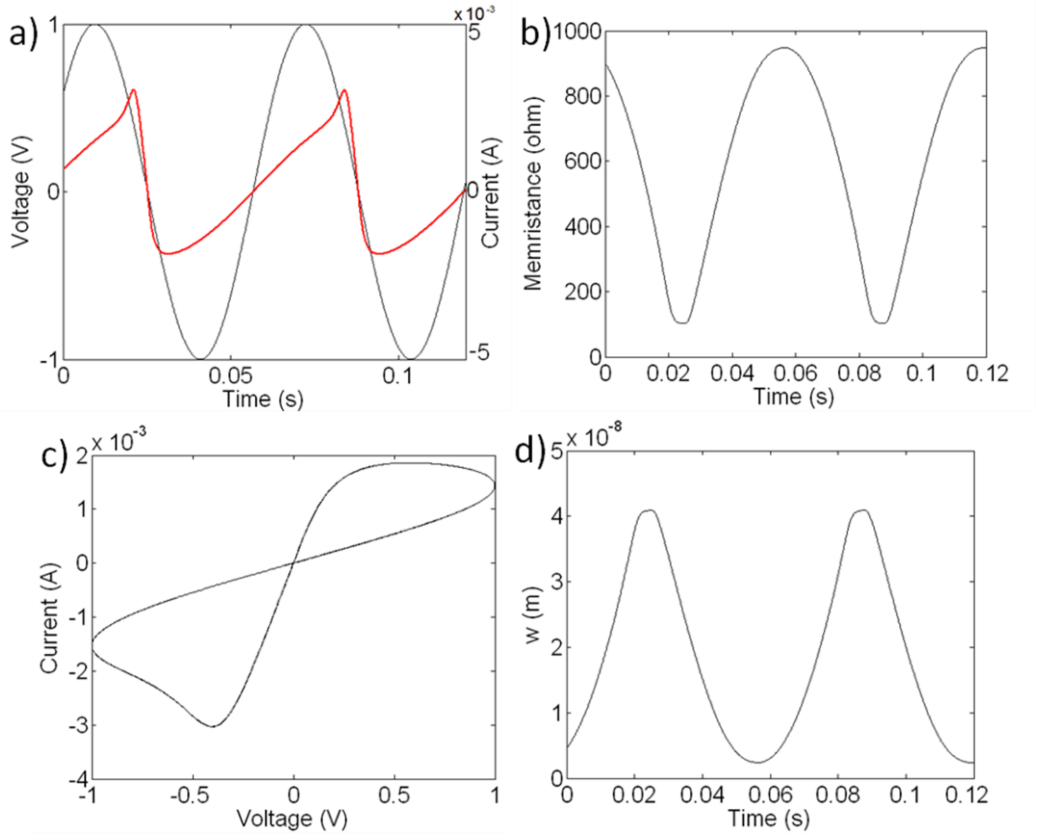


Figure 5.2.6 Figures are of a) $I(t)$ & $V(t)$, b) $w(t)$, c) V-I hysteresis behavior , and d) $M(t)$ memristor simulation results using non-linear dopant drift model and Biolek's window function, with parameters $\mu_D = 4.4 \times 10^{-13}$ $m^2 \cdot V^{-1} \cdot s^{-1}$, $D = 41$ nm, $w_0/D = 0.11$, $R_{on} = 100\ \Omega$, $r = 10$, p = 7, $v_0 = 1$ V, $\omega = 100$ rad/s, $V(t) = \sin(100\ t + 0.62)$ V, $\Phi(t) = (0.01)\ [\cos(0.62) - \cos(100\pi\ t + 0.62)]$ Wb, and $\Delta t = 10^{-4}$ sec.

5.3 Reverse Engineer Model Template

While the theoretical behavior of these devices is very regular, physical devices are rarely as exact. Accordingly, more complex models have been proposed to account for the several different switching mechanisms found in different memristive devices [3, 8, 72, 73, 89-97]. Yet, despite the various predictive models now available in the literature, only two [98, 99] have been applied to measured data and evaluated according to fitting

fidelity to an experimentally measured I-V curve from an arbitrary memristive device fabricated in the laboratory.

The intent of the boundary drift models was to describe device behavior with respect to various explicit physical parameters. The complexity of the model may increase the range of reproducible device behaviors, but it may also prove to be too difficult to determine the appropriate parameter values for an arbitrary device. Thus models based on experimental observations [99] were developed to account for irregular I-V characteristics.

The proposed empirical model was developed for use in a research environment for developing and selecting memristive devices for various circuits. Per change to a physical parameter, a new model would need to be prepared for the circuit designer. An efficient device model will have several attributes 1) follow a template format to allow for readily adaption to the different device types available, 2) provide an adequate degree of behavioral fidelity, 3) operate in a manner not computationally burdensome which will become very significant when considering large-scale simulations, and 4) function with available circuit modeling software, e.g. SPICE. It is with these ends that the Biolek boundary drift model was compared with the set of memristive device model templates that were developed.

a) Biolek Non-linear Boundary Drift Model

The Biolek model as described in Section 5.2 *c)* possessed several advantages over the other state change models. First, the model employed a non-linear boundary drift equation, which was more realistic than a first order approximation linear resistance change model. Additionally, the non-linear equation modification did not suffer from boundary effects as the Joglekar model did. Lastly, the resulting I-V curve was asymmetric which is typical of physical memristive devices.

However, this window function only applies to bipolar(+) devices. To be a general use bipolar model, bipolar(-) devices ought to be modeled as well. Thus, an additional variable $ч$ was added by the author to the Biolek window function, where $ч$ = 1 or (-1) if the memristive device switching scheme is bipolar(+) or bipolar(-), respectively. Thus Equations 5.2.23 & 5.2.24 become

$$F_p(x) = ч\left\{1 - \left[x - \mathrm{u}(I)\right]^{2p}\right\}, \tag{5.3.1}$$

where

$$\mathrm{u}(I) = \begin{cases} \frac{1+ч}{2}, \text{if } (I) \leq 0 \\ \\ \frac{1-ч}{2}, \text{if } (I) > 0 \end{cases}. \tag{5.3.1}$$

Even with expanded applicability, the use of the window function required additional calculations. Biolek, *et al.* noted that if the aforesaid window function was inadequate to describe the behavior of a particular set of devices, a new function must be developed, which may or may not prove time prohibitive.

b) Piece-wise Linear State Change Bipolar Model

The piece-wise linear (PWL) modeling approach differed in several key aspects from the previously described models. In the first place, physical parameters were not considered. Rather, an I-V plot and corresponding input signal were all that need to be referenced.

Secondly, concerning input signals, academically, sine waves were frequently used to characterize memristive devices, since such a signal would run the device through one full switching cycle. However, even Chua noted that such an I-V curve is not predictive of the devices behavior under an arbitrary signal [10]. CMOS technology today requires digital logic, thus pulse-mode operation will be required for von Neumann computing. The PWL model expects pulse mode data when assigning variables values.

Thirdly, these next three models use threshold voltages to determine switching events. With respect to the Cu_xO memristive devices tested, a threshold voltage was recognized as the dominant factor regulating resistance switching. Especially with respect to pulse-mode operation, such a discriminator will better account for the differences in device behavior when subjected to a "read" pulse instead of a "write" or "erase" pulse. Lastly, in the previous models, the SET & RESET operations were gradual. In practice, these transitions are usually abrupt [7, 46, 101]. These rapid events naturally lent themselves to a PWL modeling approach.

For the bipolar model in particular, the end resistance under both +V & -V, the SET & RESET voltages, and the time required for SET & RESET operations are used in the model, all of which may be read off of an I-V plot and corresponding voltage signal, $V(t)$.

The switching scheme, bipolar(±), was encoded in the ψ variable. While a model will enact a switch precisely at the threshold voltage, a manufactured device will switch inside a voltage window. This model allowed for such a voltage window to be encoded. Additionally, every time the device switched, a new threshold voltage was assigned to the device.

Per time step, the model performs the proceeding routine. The model first checks if the "switch_value" variable is "0", indicating that the device is either at LRS or HRS resistance, that is, not in the process of switching. If so, then the input voltage is compared to the switching voltage values. If the threshold voltage for a SET operation is applied, the "switch_value" is set to "(+1)"; conversely, if the RESET voltage is applied, the "switch_value" is set to "(-1)".

Next, for a SET assigned device

$$M(t_{i+1}) = M(t_i) - \frac{\Delta r \Delta t V(t_{i+1})}{t_{\pm} V_{\pm}}; \tag{5.3.3}$$

and for a RESET assigned device,

$$M(t_{i+1}) = M(t_i) - \frac{\Delta r \Delta t V(t_{i+1})}{t_{\mp} V_{\mp}}, \tag{5.3.4}$$

where M is the memristance, Δr is the absolute difference between LRS and HRS resistance, Δt is the time step-size, V is the applied voltage bias, $t_{\pm}$ is the time to effect a switch under $+V$ ($-V$), and $V_{\pm}$ is the threshold voltage per polarity. This procedure is iterated for the duration of the appropriate switch event, at which point, the "switch_value" is again set to "0," concluding the switching operation. See Figure 5.3.1.

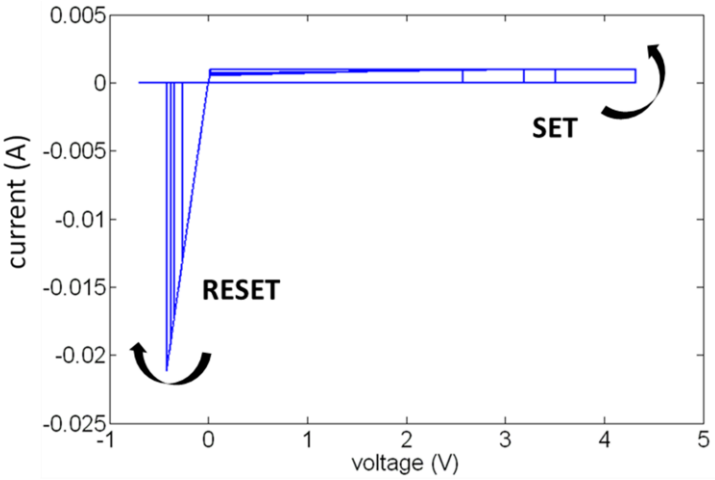


Figure 5.3.1 This figure depicts the simulation results of the piece-wise linear state change bipolar model over several cycles.

c) Piece-wise Linear State Change Unipolar Model

It was straightforward to adapt the PWL bipolar memristive device model to become a unipolar device model. The first major alteration was to multiply the applied voltage by the η variable. In this way, only the voltage polarity which incurs a switching event will be observed to be positively biased, e.g. (η= -1)*(-V) = +V. This then reduced the number of comparison steps required to effect the prescribed changes. All other operations proceed as previously described. See Figure 5.3.2.

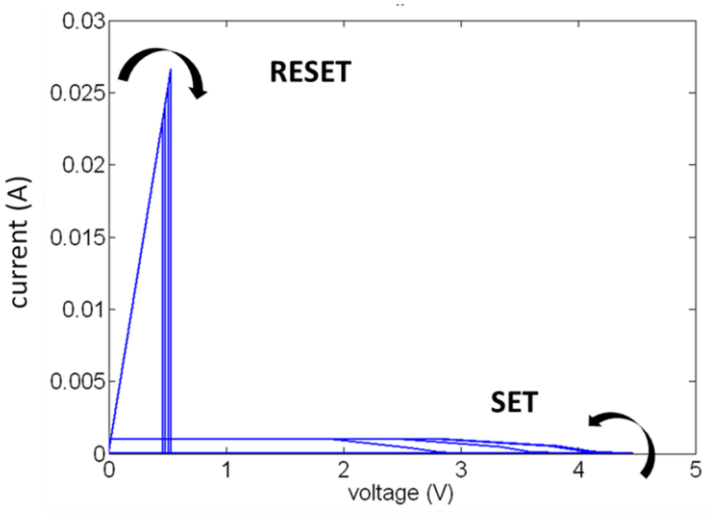


Figure 5.3.2 This figure depicts the simulation results of the piece-wise linear state change unipolar model over several cycles.

d) Piece-wise Linear State Change Nonpolar Model

Thus far, both bipolar and unipolar devices can be modeled; yet each model is mutually exclusive. To model nonpolar memristive devices, both models must be combined. For the nonpolar model, there is a V_{SET} and V_{RESET} threshold value for both $+V$ and $-V$ with corresponding required switching times t_{SET} and t_{RESET}. The model operated as otherwise described but with more comparison operations per simulation time step. See Figure 5.3.3.

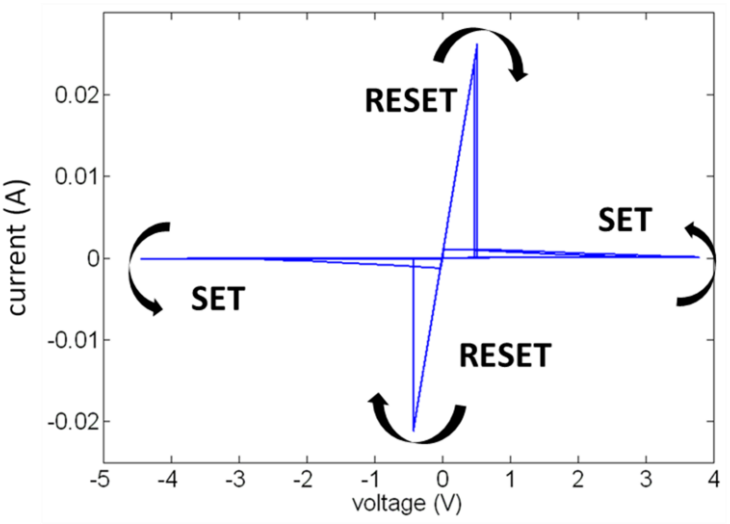


Figure 5.3.3 This figure depicts the simulation results of the piece-wise linear state change nonpolar model over several cycles.

5.4 Model Comparison

For this study only curve fidelity was considered, since computation time would best be evaluated on a SPICE program. For this comparison, an I-V curve from a silver chalcogenide and a copper oxide memristive device were used.

a) W/Ge_2Se_3/Ag_2Se/Ge_2Se_3/Ag/Ge_2Se_3/W Memristive Device I-V Curve

Bipolar(+) W/Ge_2Se_3/Ag_2Se/Ge_2Se_3/Ag/Ge_2Se_3/W memristive devices prepared by Boise State University [99] were cycled under a 10 Hz signal. Comparisons of the original plot and the subsequent fittings are shown in Figure 5.4.1 a) & b).

Since the Biolek model did not account for any threshold voltages, it started increasing the memristance as soon as the voltage bias reversed polarity. Thus it missed critical

areas of the device's behavior in the (–V) regions. In a circuit simulation, this model would then predict higher power than actually consumed per device.

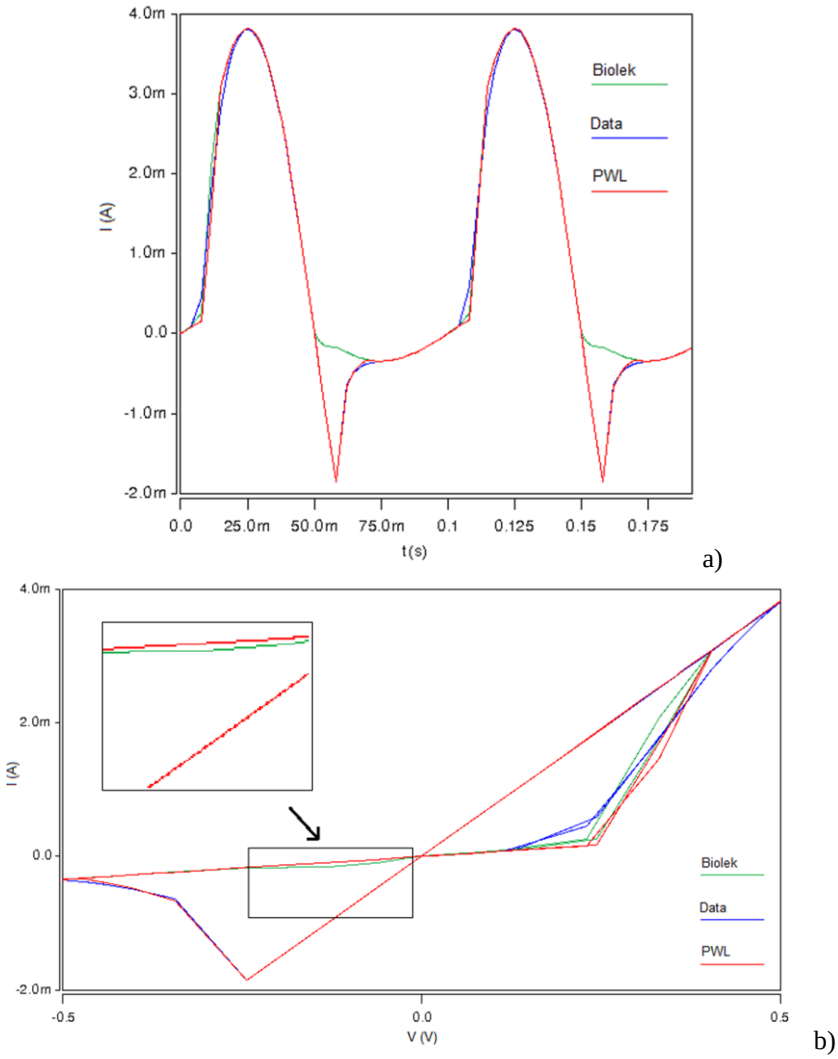


Figure 5.4.1 a) Figure depicts the current response of a chalcogenide memristive device to a 10 Hz signal. b) The model I-V plot dervived from the data in a)

b) Al/Cu$_x$O/Cu Memristive Device I-V Curve

A full bipolar- cycle of an Al/Cu$_x$O/Cu memristive device as described in Section 4.3, was also modeled (Figure 5.4.2). As opposed to the more gradual I-V in Figure 5.4.1 b), Figure 5.4.2 b) has very sharp transitions between states. This agrees well with the PWL

threshold voltage modeling assumption as opposed to a flux based summation espoused by the Biolek model.

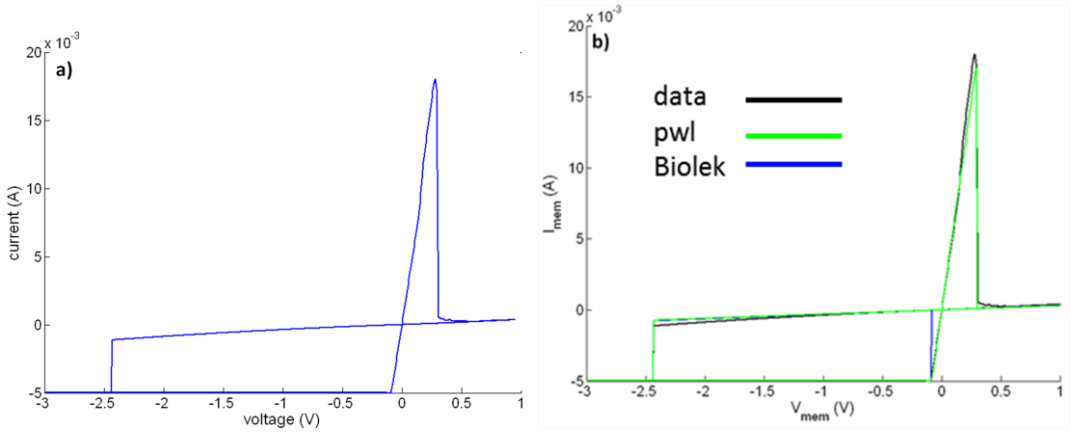


Figure 5.4.2 a) Figure depicts the I-V plot from an Al/Cu_xO/Cu memristive to be modeled . b) The derived models were overlain on a).

Additionally, in practice, a current limit was imposed during the SET step to prevent the device from breaking. This "current compliance" was not used during RESET. Thus, when modeling these particular devices a current limiting resistor or transistor must be included to accurately model the device. In this case, current compliance was forced upon the model in the code explicitly. Figure 5.4.2 b) displays the fit with the current compliance forced in the model.

As in the previous case, there was significant dissimilarity between the Biolek model and the data, in this case over the +V bias. The Biolek model predicted a RESET in the SET region and thus persisted at R_{off} over the entirety of +V. For both experimental data sets, the Biolek model required a new window function to accurately replicate the data.

Of the two memristive device models compared in this manner, the PWL was more advantageous than the Biolek model for the purposes of recreating an arbitrary memristive device I-V curve. The PWL model could account for threshold voltage values and several different switching schemes. These results of course do not preclude the use of the Biolek model as a general purpose modeling framework, but as was demonstrated, a means of readily selecting an appropriate window function would be required.

5.5 Summary

Memristive device models have been developed with two different purposes. The first purpose was the scientific model, which accounted for various physical parameters. The second merely sought to recreate what was there without accounting for why it was so. While the former may have been more elegant, this approach did not prove a viable method to create device models for circuit modeling software programs.

General purpose empirical models of completely nonpolar memristive devices were developed to meet the need for adaptable device models to facilitate rapid prototyping of circuits with experimental memristive devices. These models afforded greater data recreation fidelity than the physics based model. Additionally, these empirical models were successfully employed to model data collected from memristive devices of widely differing material compositions.

VIII. Conclusion

It has been shown that memristive devices are a novel technology and may have significant role in future CMOS circuit design. Their potential applications are diverse from von Neumann computing to neuromorphic computing. Since bistable switching has been reported for a variety of semiconductor industry authorized materials, there exists a wide range of possible material stack combinations from which to make memristive devices.

Copper oxide was studied as the insulating layer of a MIM memristive device because of the already pervasive use of copper in a CMOS foundry, the myriad of ways available to oxidize copper, and the increased application space of nonpolar device switching. This research focused on Al/Cu_xO/Cu memristive devices, where the Cu_xO was grown via plasma oxidation

As was shown, these devices demonstrated consistent, complete nonpolar behavior with operating voltages typically within |3| V and required currents under 20 mA. These operating parameters are acceptable for use in CMOS circuitry. The switching mechanism of these devices was determined to be via a conductive filament. This knowledge directly led to a patent application for a hardware based random bit generator using these devices cycled in a lateral fashion.

Physical and empirical models of these devices were created for MATLAB, HSPICE,& Verilog A environments. While the physical model proved of limited practical

consequence, the robust empirical model allows for rapid prototyping of CMOS-memristor circuitry.

This research is expected to continue beyond this thesis. CMOS digital logic operates via voltage pulses and not voltage sweeps. While voltage sweeps are more informative for characterizing memristive devices than pulse mode operation, it would be best to evaluate these memristive devices in a manner akin to their planned use. Such a study would characterize these devices using a wide range of voltage magnitudes, polarities, and pulse widths.

The lateral switching phenomena is also expected to be studied further, primarily pursuing the experiment concerning filament growth as described in Section 4.5. On a related front, the switching mechanism of these devices ought to be nonsusceptible to radiation damage [102], but this would need to be experimentally verified. These results would prove useful in any future device engineering work.

Lastly, these devices are expected to be evaluated for use in neuromorphic computing learning circuits. Several learning circuits have already been developed and tested with memristive devices. It would thus be of great interest to compare the "learning" results of a circuit using different memristive devices.

References

[1] B. Hayes, “The Memristor,” *American Scientist*, Vol. 99, pp. 106-110 (2011).

[2] H. Akinaga, H. Shima, “Resistive Random Access memory (ReRAM) Based on Metal Oxides,” *Proceedings of the IEEE*, Vol.98, No.12, pp.2237-2251 (2010).

[3] D. Strukov, G. Snider, D. Stewart and R. Williams, "The missing memristor found," *Nature*, Vol. 453, pp. 80-83 (2008).

[4] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, “Nanoscale Memristor Device as a Synapse in Neuromorphic Systems,” *Nano Lett.*, 10, pp. 1297 (2010).

[5] R. Dong, D. S. Lee, W. F. Xiang, S. J. Oh, D. J. Seong, S. H. Heo, H. J. Choi, M. J. Kwon, S. N. Seo, M. B. Pyun, M. Hasan, and H. Hwang, “Reproducible hysteresis and resistive switching in metal-CuxO-metal heterostructure,” *Appl Phys Let.*, Vol. 90, p. 042107 (2007).

[6] A. Chen, S. Haddad, Y. C. Wu, Z. Lan, T. N. Fang, and S. Kaza, “Switching characteristics of Cu_2O metal-insulator-metal resistive memory,” *Appl. Inst. Phys.*, Vol. 91, p. 123517 (2007).

[7] H. B. Lv, P. Zhou, X. F. Fu, M. Yin, Y. L. Song, L. Tang, T. A. Tang, and Y. Y. Lin, “Polarity-Free Resistive Switching Characteristics of CuxO Films for Non-volatile Memory Applications,” *Chi. Phys. Lett.*, Vol. 25, No. 3, p. 1087 (2008).

[8] L. Chua, "Memristor - The Missing Circuit Element," *IEEE Transactions on Circuits Theory (IEEE)*, Vol. 18, No. 5, pp. 507–519 (1971).

[9] L. Chua and S. M. Kang, “Memristive Device and Systems,” *Proceedings of IEEE*, Vol. 64, No. 2, pp. 209-223 (1976).

[10] L. Chua, “Resistance switching memories are memristors,” *Applied Physics A*, Vol. 102, pp. 765-783 (2011).

[11] M. T. Hickmott, “Low-frequency negative resistance in thin anodic oxide films,” *J. Appl. Phys.* Vol. 33, pp. 2669–2682 (1962).

[12] G. Dearnaley, A. M. Stoneham, and D. V. Morgan, “Electrical phenomena in amorphous oxide films,” *Rep. Prog. Phys.* Vol. 33, pp. 1129–1192 (1970).

[13] Y. Hirose, “Polarity-dependant memory switching and behavior of Ag dendrite in Ag-photodoped amorphous As_2S_3 films,” *J. Appl. Phys.*, Vol. 47, No. 6, p. 2767 (1976).

[14] R. S. Potember, T. O. Poehler, D. O. Cowan, “Electrical switching and memory phenomena in Cu-TCNQ thin films,” *Appl. Phys. Lett.*, Vol. 34, No. 6, p. 405 (1979).

[15] A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel, D. Widmer, “Reproducible switching effect in thin oxide films for memory applications,” *Applied Physics Letters*, Vol. 77, No. 1, p. 140 (2000).

[16] C. P. Collier, G. Mattersteig, E. Wong, Y. Luo, K. Beverly, J. Sampaio, F. Raymo, J. Stoddart, J. Heath, “A [2]catenane-based solid state electronically reconfigurable switch,” *Science,* Vol. 289, pp. 1172–1175 (2000).

[17] C. Rossel, G. I. Meijer, D. Bre’maud, and D. Widmer, “Electrical current distribution across a metal-insulator-metal structure during bistable switching,” *J. Appl. Phys.*, Vol. 90, No. 6, p. 2892 (2001).

[18] X. Duan, Y. Huang, and C. Lieber, “Nonvolatile Memory and Programmable Logic from Molecule-Gated nanowires,” *Nano Lett.*, Vol. 2, No. 5, p. 487 (2002).

[19] P. van der Sluis, “Non-volatile memory cells based on $ZnxCd_{1-x}S$ ferroelectric Schottky diodes,” *Appl. Phys. Lett.*, Vol. 82, No. 23, p. 4089 (2003).

[20] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D. S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I/ S. Byun, J. S. Choi, and B. H. Park, “Reproducible resistance switching in polycrystalline NiO films,” *Appl. Phys. Lett.*, Vol. 85, No. 23, p. 5655 (2004).

[21] D. R. Stewart, D. A. A. Ohlberg, P. A. Beck, Y. Chen, R. S. Williams, J. O. Jeppesen, K. A. Nielsen, and J. F. Stoddart, “Molecule-independent electrical switching in Pt/organic monolayer/Ti devices,” *Nano Lett.*, Vol. 4, No. 1, pp. 133–136 (2004).

[22] T. Oka and N. Nagaosa, “Interfaces of Correlated Electron Systems: Proposed Mechanism for Colossal Electroresistance,” *Phys. Rev. Lett.*, Vol. 95, p. 266403 (2005).

[23] M. N. Kozicki, M. Park, and M. Mitkova, “Nanoscale memory elements based on solid-state electrolytes,” *IEEE Trans. Nanotechnol.*, Vol. 4, pp. 331–338 (2005).

[24] C. A. Richter, D. R. Stewart, D. A. A. Ohlberg, and R. S. Williams, “Electrical characterization of Al/AlO_x/molecule/Ti/Al devices,” *Appl. Phys. Mater. Sci. Process.*, Vol. 80, pp.1355-1362 (2005).

[25] J. H. A. Smits, S. C. J. Meskers, R. A. J. Janssen, A. W. Marsman, and D. M. de Leeuw, “Electrically rewritable memory cells from poly(3-hexylthiophene) Schottky diodes,” *Adv. Mater.*, Vol. 17, pp.1169–1173 (2005).

[26] K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," *Nature*, Vol. 433, pp. 47–50 (2005).

[27] M. Hamaguchi, K. Aoyama, S. Asanuma,Y. Uesu, and T. Katsufuji, "Electric-field induced resistance switching universally observed in transition-metal-oxide thin films," *Appl. Phys. Lett.*, Vol. 88, p. 142508 (2006).

[28] S. Karthäuser, B. Lüssem, M. Weides, M. Alba, A. Besmehn, R. Oligschlaeger, and R. Waser, "Resistive switching of rose Bengal devices: a molecular effect?," *J. Appl. Phys.*, Vol. 100, No. 9, p. 094504 (2006).

[29] Q. X. Lai, Z. H. Zhu, Y. Chen, S. Patil, and F. Wudl, "Organic nonvolatile memory by dopant-configurable polymer," *Appl. Phys. Lett.*, Vol. 88, p. 133515 (2006).

[30] R. Oligschlaeger, R. Waser, R. Meyer, S. Karthauser, and R. Dittmann, "Resistive switching and data reliability of epitaxial (Ba,Sr)TiO_3 thin films," *Appl. Phys. Lett.*, Vol. 88, p. 042901 (2006).

[31] A. Sawa, T. Fujii, M. Kawasaki, and Y. Tokura, "Interfaces resistance switching at a few nanometer thick perovskite manganite layers," *Appl. Phys. Lett.*, Vol. 88, p. 232112 (2006).

[32] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single crystalline $SrTiO_3$," *Nature Mater.*, Vol. 5, pp. 312–320 (2006).

[33] J. J. Blackstock, W. F. Stickle, C. L. Donley, D. R. Stewart, R. S. Williams, "Internal structure of a molecular junction device: chemical reduction of PtO_2 by Ti evaporation onto an interceding layer," *J. Phys. Chem. C*, Vol. 111, pp. 16–20 (2007).

[34] S. Dietrich, M. Angerbauer, M. Ivanov, D. Gogl, H. Hoenigschmid, M. Kund, C. Liaw, M. Markert, R. Symanczyk, L. Altimime, S. Bournat, and G. Mueller, "A nonvolatile 2-Mbit CBRAM memory core featuring advanced read and program control," *IEEE J. Solid State Circuits*, Vol. 42, pp. 839–845 (2007).

[35] J. R. Jameson, Y. Fukuzumi, Z. Wang, P. Griffin, K. Tsunoda, G. I. Meijer, and Y. Nishi, "Field-programmable rectification in rutile TiO2 crystals," *Appl. Phys. Lett.*, Vol. 91, p. 112101 (2007).

[36] D. S. Jeong, H. Schroeder, and R. Waser, "Coexistence of bipolar and unipolar resistive switching behaviors in a Pt/TiO_2/Pt stack," *Electrochem. Solid State Lett.*, Vol. 10, G51–G53 (2007).

[37] J. C. Scott and L. D. Bozano, "Nonvolatile memory elements based on organic materials," *Adv. Mater.*, Vol. 19, pp. 1452–1463 (2007).

[38] N. B. Zhitenev, A. Sidorenko, D. M. Tennant, and R. A. Cirelli, “Chemical modification of the electronic conducting states in polymer nanodevices,” *Nature Nanotechnol.*,Vol. 2, pp. 237–242 (2007).

[39] R. Waser and M. Aono, “Nanoionics-based resistive switching memories,” *Nature Mater.*, Vol. 6, pp. 833–840 (2007).

[40] Y. Dong, G. Yu, M. McAlpine, W. Liu, and C. Lieber, “Si/a-Si core/Shell Nanowires as nonvolatile Crossbar Switches,” *Nano Letters*, Vol. 8, No. 2, p. 386 (2008).

[42] D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, “Atomic structure of conducting nanofilaments in TiO2 resistive switching memory,” *Nature Nanotechnology*, Vol. 5, pp. 148-153 (2010).

[41] S. Williams, “How We Found the Missing Memristor,” *IEEE Spectrum*, Vol. 45, No. 12, pp. 28-35 (2008).

[43] H. B. Lv, M. Yin, X. F. Fu, Y. L. Song, L. Tang, P. Zhou, T. A. Tang, B. A. Chen, and Y. L. Lin, “Resistive Memory Switching of Cu_xO Films for a Nonvolatile Memory Application,” *IEEE Electron Device Letters*, Vol. 29, No. 4, pp. 309-311 (2008).

[44] S.O. Kang, S. Hong, J. Choi, J.S. Kim, I. Hwang, I.S. Byun, K.S. Yun, B. H. Park, “Electrochemical growth and resistive switching of flat-surfaced and (111)-oriented Cu_2O films,” *Appl. Phys. Lett.*, Vol. 95, p. 092108 (2009).

[45] M. Di Ventra, Y. V. Pershin, L. O. Chua, “Circuit Elements With Memory: Memristors, Memcapacitors, and Meminductors,” *Proc. IEEE*, Vol. 97, pp. 1717-1724 (2009).

[46] A. Chen; S. Haddad, Y.C. Wu, T.N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, M. Taguchi, "Non-volatile resistive switching for advanced memory applications," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp.746-749 (2005).

[47] R. Dong, D. S. Lee. W. F. Xiang, S. J. Oh, D. J. Seong, S. H. Heo, H. J. Choi, M. J. Kwon, S. N. Seo, M. B. Pyun, M. Hasan, and H. Hwang, “Repoducible hysteresis and resistive switching in metal-CuxO-metal heterostructures,” *Appl. Phys. Lett.*, Vol. 90, p. 042107 (2007).

[48] H. B. Lv, M. Yin, Y. L. Song, X. F. Fu, L. Tang, P. Zhou, C. H. Zhao, T. A. Tang, B. A Chen, and Y. Y. Lin, “Forming Process Investigation of CuxO Memory Films,” *Electron Device Letters, IEEE*, Vol. 29, No.1, pp. 47-49 (2008).

[49] C. H. Kim, Y. H. Jang, H. J. Hwang, Z. H. Sun, H. B. Moon, and J. H. Cho, "Observation of bistable resistance memory switching in CuO thin films," *Appl. Phys. Lett.*, Vol. 94, p. 102107 (2009).

[50] A. Chen, S. Haddad, Y. C. Wu, T. N. Fang, S. Kaza, and Z. Lan, "Erasing characteristics of Cu_2O metal-insulator-metal resistive switching memory," *Appl. Phys. Lett.*, Vol. 92, p. 013503 (2008).

[51] S. M. Bishop, H. Bakhru, S. W. Novak, B. D. Briggs, R. J. Matyi, and N. C. Cady, "Ion implantation synthesized copper oxide-based resistive memory devices," *Appl. Phys. Lett.*, Vol. 99, p. 202102 (2011).

[52] S. M. Bishop, B. D. Briggs, Z. P. Rice, S. Addepalli, N. R. McDonald and N. C. Cady, "Fabrication and Characterization of Copper Oxide Resistive Memory Devices," *MRS Proceedings 2011*, p. 1337 (2011).

[53] W. Wang, T. T. Jing, B. Butcher, "FPGA based on integration of memristors and CMOS devices," *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp. 1963-1966 (2010).

[54] A. Sawa, "Resistive switching in transition metal oxides," *Mater. Today*, Vol. 11, pp. 28-36 (2008).

[55] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor–CMOS Hybrid Integrated Circuits for Reconfigurable Logic," *Nano Lett.*, Vol. 9, p. 3640 (2009).

[56] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, Vol. 464, pp.873-876 (2010).

[57] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature Materials*, Vol. 9, pp. 403-406 (2010).

[58] J. G. White, E. Southgate, J. N. Thomson, and S. Brenner, "The Structure of the Nervous System of the Nematode Caenorhabditis elegans," *Phil. Trans. R. Soc. Lond. B*, Vol. 314, No. 1165, pp. 1-340 (1986).

[59] K. Eshraghian, K. R. Cho, O. Kavehei, S. K. Kang, D. Abbott, S. M. S. Kang, "Memristor MOS Content Addressable Memory (MCAM): Hybrid Architecture for Future High Performance Search Engines," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, Vol. 19, No. 8, pp. 1407-1417 (2011).

[60] K. H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, and W. Lu, "A Functional Hybrid Memristor Crossbar-Array/CMOS System for

Data Storage and Neuromorphic Applications," *Nano Lett.*, Vol. 12, pp. 389-395 (2012).

[61] G. H. Kim, K. M. Kim, J. Y. Seok, M. H. Lee, S. J. Song, and C. S. Hwang, "Influence of the Interconnection Line Resistance and Performance of a Resistive Cross Bar Array Memory," *J. Electrochem. Soc.*, Vol. 157, No. 10, G211-G215 (2010).

[62] J. von Neumann, "First draft of a report on the EDVAC, (June 1945)," reprinted with corrections in the *Annals of the History of Computing*, Vol. 15, pp. 25-75 (1993).

[63] A. Bofill and A. F. Murray, "Circuits for VLSI implementation of temporally asymmetric Hebbian learning," *Advances in Neural Information processing systems*, Vol. 14, Eds. T. G. Dietterich, S. Becker, and Z. Ghahramani, editors, MIT Press, Cambridge, MA (2001).

[64] J. V. Arthur and K. Boahen, "Learning in Silicon: Timing is Everything," *Advances in Neural Information Processing Systems*, Vol. 18, Eds. B. Sholkopf and Y. Weiss, MIT Press (2006).

[65] G. Indiveri, E. Chicca, and R. Douglas. "A VLSI array of lowpower spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Transactions on Neural Networks*, Vol. 17, pp. 211-221 (2006).

[66] J. Schemmel, K. Meier, E. Mueller, "A new VLSI model of neural microcircuits including spike time dependent plasticity," *Proc. ESANN2004*, pp. 405-410 (2004).

[67] B. Glackin, T.M. McGinnity, L.P. Maguire, QX Wu, A. Belatreche, "A novel approach for the implementation of large scale spiking neural networks on FPGA hardware," *Proc. IWANN 2005 Computational Intelligence and Bioinspired Systems*, pp.552-563, (2005).

[68] R.J. Vogelstein, U. Malik, G. Cauwenberghs, "Silicon spikebased synaptic array and address-event transceiver," *Proceedings of ISCAS04*, Vol. 5, pp. 385-388 (2004).

[69] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," (2009) [Online]. Available: http://arXiv.org/abs/arXiv:0905.2935

[70] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, "Memristive model of amoeba's learning," *Phys. Rev. E*, Vol. 80, p. 021926 (2009).

[71] H.B. Lv, M. Yin, X.F. Fu, Y.L. Song, L. Tang, P. Zhou, C.H. Zhou, T.A. Tang, B.A. Chen, and Y.Y. Lin, "Resistive Memory Switching of Cu_xO Films for a

Nonvolatile Memory Application," *IEEE Electron Device Lett.*, Vol. 29, No. 4, pp. 309-311 (2008).

[72] Y. Joglekar and S. Wolf, "The elusive memristor: properties of basic electrical circuits," *Eur. J. Phy.*, Vol. 30, pp. 661–675 (2009).

[73] Z. Biolek, D. Biolek, and V. Biolková, "Spice Model of Memristor with Nonlinear Dopant Drift," *Radioengineering*, Vol. 18, No. 2, pp. 210-214. (2009).

[74] A. E. Rakhshani, "The role of space-charge-limited-current conduction in evaluation of the electrical properties of thin Cu_2O films," *J. Appl. Phys*, Vol. 69, p. 2365 (1991).

[75] A. E. Rakhshani, "Thermostimulated impurity conduction in characterization of electrodeposited Cu_2O films," *J. Appl. Phys*, Vol. 69, p. 2290 (1991).

[76] M A Lampert, "Volume-controlled current injection in insulators," *Rep. Prog. Phys*,.Vol. 27, p. 329 (1964).

[77] W.Y. Yang and S.W. Rhee, "Effect of electrode material on the resistance switching of Cu_2O film," *Appl. Phys. Lett.*, Vol. 91, p. 232907 (2007).

[78] G. F. Alapatt, W. R. Harell, Y. Freeman, P. Lessner, "Observation of the Poole-Frenkel Effect in Tantalum Polymer Capacitors," *IEEE Southeast Con 2010*, pp. 498-501 (2010).

[79] Y. C. Yang, F. Pan, Q. Llu, M. Llu, F. Zeng, "Fully Room-Temperature-Fabricated Nonvolatile Resistive Memory for Ultrafast and High-Density Memory Application," *Nano Lett.*, Vol. 9, No. 4, pp. 1636-1643 (2009).

[80] Q. Liu, M. Liu, Y. Wang, H. Lv, S. Long, and W. Wang, "Doping technology: An effective way to improve the performances of resistive switching memory," *Junction Technology (IWJT), 2011 11th International Workshop on* , pp.80-83 (2011).

[81] F. Miao, W. Yi, I. Goldfarb, J. J. Yang, M. X. Zhang, M. D. Pickett, J. P. Strauchan, G. Medeiros-Ribeiro, and R. S. Williams, "Continuous Electrical Tuning of the Chemical Composition of TaO_x-Based Memristors," *ACS Nano*, Vol. 6, No. 3, pp. 2312-2318 (2012).

[82] C. J. Li, S. Jou, and W. L. Chen, "Effect of Pt and Al Electrodes on Resistive Switching Properties of Sputter-Deposited Cu-Doped SiO_2 Film," *Jpn. J. Appl. Phys.*, Vol. 50, 01BG08 (2011).

[83] N. Bellakhal, K. Draou, B.G. Cheron, J.L. Brisset, "Electrochemical investigation of copper oxide films formed by oxygen plasma treatment," *Mater. Sci. Eng. B*, Vol. 41, No. 2, pp. 206-216 (1996).

[84] P. Zhou, H.B. Lv, M. Yin, L. Tang, Y.L. Song, T.A. Tang, Y.Y. Lin, A. Bao, A.Wu, S. Cai, H. Wu, C. Liang, M.H. Chi, "Performance improvement of CuOx with gradual oxygen concentration for nonvolatile memory application," *J. Vac. Sci. Technol. B Microelectron Nanometer Struct.*, Vol. 26, No. 3, pp. 1030-1032 (2008).

[85] K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, "Anode-interface filamentary mechanism in resistive switching of TiO2 thin films," *Appl. Phys. Lett.*, Vol. 91, p. 012907 (2007).

[86] J. L. Brady, "Limitations of True Random Number Generator in a field programmable gate array," AFIT (2007).

[87] D. Ielmini, "Universal Reset Characteristics m of Unipolar and Bipolar Metal-Oxide RRAM," *IEEE Transactions on Electron Devices*, Vol. 58, No. 10, pp. 3246–3253 (2011).

[88] M. Pickett, D. Strukov, J. Borghetti, J. Yang, G. Snider, D. Stewart, and R. Williams, "Switching dynamics in titanium dioxide memristive devices," *J. Appl. Phys.*, Vol. 106, No. 7, p. 074508 (2009).

[89] S. Benderli, T.A. Wey, "On SPICE macromodelling of TiO_2 memristors," *Electronics Letters*, Vol. 45, No. 7, pp. 377-379 (2009).

[90] Y. Chen, X. Wang, "Compact modeling and corner analysis of spintronic memristor," *Nanoscale Architectures, IEEE/ACM International Symposium on*, pp. 7-12, (2009).

[91] Y. Ho, G.M. Huang, and P. Li, "Nonvolatile memristor memory: Device characteristics and design implications," *Computer-Aided Design - Digest of Technical Papers, 2009. ICCAD 2009. IEEE/ACM International Conference on*, pp. 485-490 (2009).

[92] D. Strukov and R. Williams, "Exponential ionic drift: fast switching and low volatility of thin-film memristors," *App. Phys. A*, Vol. 94, No. 3, pp. 515-519 (2009).

[93] W. Wang, Q. Yu, C. Xu, and Y. Cui, "Study of filter characteristics based on PWL memristor," *Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on*, pp. 969-973 (2009).

[94] D. Wang, Z. Hu, X. Yu; and J. Yu, "A PWL model of memristor and its application example," *Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on*, pp. 932-934 (2009).

[95] D. Batas and H. Fiedler; "A Memristor Spice Implementation and a New Approach for Magnetic Flux Controlled Memristor Modeling," *Nanotechnology, IEEE Transactions on*, Vol. 10, No. 2, pp. 250-255 (2010).

[96] H. Li and M. Hu, "Compact model of memristors and its application in computing systems," *Design, Automation & Test in Europe Conference & Exhibition, 2010*, pp. 673-678 (2010).

[97] D. Niu, Y. Chen, and Y. Xie, "Low-power dual-element memristor based memory design," *Low-Power Electronics and Design (ISLPED), 2010 ACM/IEEE International Symposium on*, pp. 25-30 (2010).

[98] N. Gilbert, C. Gopalan, and M. Kozicki, "A macro model of programmable metallization cell devices," *Solid-State Electronics*, Vol. 49, No. 11, pp. 813-1819 (2005).

[99] Pino, R.E.; Bohl, J.W.; McDonald, N.; Wysocki, B.; Rozwood, P.; Campbell, K.A.; Oblea, A.; Timilsina, A., "Compact method for modeling and simulation of memristor devices: Ion conductor chalcogenide-based memristor devices," *Nanoscale Architectures (NANOARCH), 2010 IEEE/ACM International Symposium on*, pp. 1-4 (2010).

[100] H. A. Miley, "Copper Oxide Films," *J. Am. Chem. Soc.*, Vol. 59, No. 12, pp. 2626–2629 (1937).

[101] L. Lin, T.H. Hou, J. Shieh, J.H. Lin, C.T. Chou, and Y.J. Lee, "Electrode Dependence of Filament Formation in HfO_2 Resistive-switching Memory", *J. Appl. Phys.*, Vol. 109, p. 084104 (2011).

[102] W. M. Tong, J. J. Yang, P. J. Kuekes, D. R. Stewart, R. S. Williams, E. DeIonno, E. E. King, S. C. Witczak, M. D. Looper, and J. V. Osborn, "Radiation Hardness of TiO2 Memristive Junctions," *Nuclear Science, IEEE Transactions on*, Vol. 57, No. 3, pp. 1640-1643 (2010).

List of Acronyms

BE	bottom electrode(s)
BEOL	back-end-of-line
CMOS	complimentary metal-oxide-semiconductor
CMP	chemical mechanical planarization
CNSE	College of Nanoscale Science & Technology, SUNY at Albany
CVD	chemical vapor deposition
DRAM	dynamic random-access memory
ECD	electrochemical deposition
FEOL	front-end-of-line
HP	Hewlett Packard
HRS	high resistance state
ICP	inductively coupled plasma
LRS	low resistance state
MIM	metal-insulator-metal
PF	Poole-Frenkel
POX	plasma oxidation
PVD	physical vapor deposition
RIE	reactive in etch
RRAM	resistive random access memory
SIMS	secondary ion mass spectrometry
SRAM	static random-access memory
SWaP	size, weight, and power
TE	top electrode(s)
TEM	transmission electron microscopy
VLSI	very-large-scale integration
XPS	X-ray photoelectron spectroscopy